International Journal of Engineering Technology and Applied Science

(ISSN: 2395 3853), Vol. 7 Issue 2 February 2021

Designing of Multiplier based on Hybrid Adder design using Wallace Tree Scheme

Mohini Yadav[1], Balram Yadav[2], Anshuj Jain[3]
[123]Dept. of Electronics & Communication Engineering, Scope College of Engineering, Bhopal, India
Mohiniy1402@gmail.com[1], balram.ieju@gmail.com[2]

Abstract- As multiplier consumes some power and as well as require some area in memory so we must require a low-power, smaller area and higher speed multiplier design. In convention multiplier the process of multiplication is quite slow as it done in several stages like partial product generation and accumulation of these products as it take some time and also consume an amount of power. The Partial product reduction and fast addition can improve the system performance. At low radix the performance of system is better and power consumption of system is quite low but as we increase the radix the performance is poor as compare to lower one to overcome this a technique is proposed which improve the performance and power consumption on conventional deign. To implement such type of design we make an analysis on different adder architecture and compare their results then select best of the them. As various multiplication techniques are available which design the radix-8 and radix-16 multiplier by using radix-4 technique. In our work we make a technique which provides us a power efficient multiplier design and the proposed multiplier shows 76.72% less power consumption as compare to existing multiplier using RC adder and also shows 62.06% less power consumption as modified multiplier using SQRT CSL adder cell.

KEYWORDS: Wallace Tree, SQRT CSL, RC, CSA, CLA, Multiplier.

I. INTRODUCTION

Every day integrated circuit technology gets additional advancement in style and performance. A faster style which consumes low power and smaller space is implied for trendy electronics styles. As advancement is done which help us to make proper utilization of energy, inscribe information and communicate info. From these technologies some of them techniques provide low power consumption design which are useful in several of applications [2-3]. In many of applications, digits and numbers are basically used for calculation, as in multiplier it is quite essential for calculation. Multipliers usually basic component in circuits which takes large space and consume a quality of power. Thence low power number multiplying design style is demanding in VLSI system style [1] [6]. New techniques are developing to make low power multipliers on technological advances, physical, circuits and logical levels. As the bit is slow processing element in digital circuit, the output of system can be determined by partial products which also define system performance, addition in the multipliers are important element in a style itself [4-5]. Therefore, optimizing the speed and space of any number is difficult task now a day. However, the space and speed range of the unit sometimes conflicting constraints as the speed increase which results in increment in Area. As circuit area and power consumption are linearly related to each other so we must make compromise between them, as speed of the system for a bigger improvement in reduction of power and space.

This section of paper discuss the introduction about the topic and rest of the paper describe as follows, section II discusses the multiplier design, and review of literature present in the section III, section IV discusses the proposed methodology and simulation results and conclusion of the paper discusses in the section V and VI respectively.

II. MULTIPLIER DESIGN

Multiplication process is done in following basic steps: firstly partial products are generated (PPG), then partial product reduction (PPR) and possibly at the top adding Carry propagate (CPA). Normally, we have combined and provide numbers for implementations ordered. As we have a tendency to surface unity that penetrates into the combinable case only in the mind, since the dimensions of integration are currently cultivated enough to begin with accommodating parallel number applications in circuits [7-8]. Every multiplication algorithms have different technique for multiplication process which include PPG, PPR and addition, The algorithm is for reduction of partial products and also for reduction of area as well as delay, from them one operand is to be recorded on high radix set.

We make an analysis on higher radix which has a set of digits given for PPG and for PPR, two methodologies are implemented, one of them is row based reduction which is done by considering an adder, another is column based reduction which can be done by considering a counter array. In execution the process addition requires a fast adder arrangement for quick result because it is on the critical path. In some times the final addition result is vary when we keep redundant results from partial products into consideration for further arithmetic operations.

III. REVIEW OF LITERATURE

Here we discuss methodologies that are similar to our works and provide solution for minimizing the power optimization of circuit. Here power and system performance of different techniques are compared. The key's to show energy and delay tradeoff for several totally various optimizing techniques together. In

microprocessors and digital process implementations we require the computation of number operation. Specifically, speed, space and low power multiplication implementation is a difficult task. Some existing techniques are available which minimize the dynamic power of circuit.

In general, there are serial and combinable number implementations. In this, multiplication process includes three steps are done namely PPG, PPR and at last step carry propagate addition. In this work a combined technique is used and as a result of the dimensions of integration now's we must accept that multiple techniques are taken into consideration for digital VLSI systems.

Nandan K. S. et al. [1]: This paper presents a clear approach to reducing CSL adder architecture area, delays and power. The typical CSL adder have drawback of high power usage and more chip areas. A small power, smaller delay and minimized area have become available for the changed SQRT CSL adder using CB logic than any other adder structure. New technologies can be designed to reduce power usage. Additional constraints may be optimized such as size, gate clock number, width and more. The results are evaluated for such constraints as area, delay and power. These are the essential constraints.

K. Tsoumanis et al, [2]: Proposes pre encoded radix-4 multiplier based on on-off encoding with extend to non-redundant radix-4 signed digit(NR4SD) encoding. NR4SD algorithm provides better results as compare to conventional BM .With NR4SD technique the numbers of generated partial products are decrease and hence the system operation performance is increased and power consumption of circuit is reduced.

Balakumaran R et al, [3]: Proposed a method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid CLA adder. MB algorithm provide less delay and low power multiplier as compare to conventional Booth and it also reduce the numbers of PP. Here CLA adder is introduce for maintaining the MAC delay. The reversible logic is used for reduction of complexity of circuit, minimizing power consumption of circuit and loss of knowledge. Here we make a survey on doable ways in which to form a FA style using completely different reversible logic gates.

Liangyu Qian et al, [4]: They present the planning of associate approximate number; this approximate multiplier consists of an approximate Booth encoder, an approximate 4-2 compressor and an approximate tree structure. The proposed approach also implemented for 8-bit, 16-bit and also applicable for 32-bit signed multiplication schemes with focusing on embedded systems applications. Simulation results compared with a particular Wallace-Booth number also as different approximate multipliers found within the technical literature, the planned approximate theme achieves important enhancements in area, delay, power consumption, and combined metrics.

Kiamal Pekmestzi et al, [5]: Presented an approach with 2's complement representation, this representation widely used as compared to other, signed number systems provide an advantage of single representation of zero as well as simple addition. Signed magnitude is used in signaling applications for representing the signal for low power analysis. Also 1's compliment is better for representation as it is easy to make conversion between signed magnitude and them. Therefore, for this system we should analysis various efficient arithmetic design. In this proposed work 1's complement Booth multiplier is proposed which having similar complexity level as of 2's complement.

Honglan Jiang et al, [6]: In this approximate design of radix-8 the architecture consist of ABM1 and ABM2, here we use truncation technique which helps us in reduction of time and power of system. The data processing with help of Wallace tree is then taken into consideration for fast addition of PP, which results speed of operation is increased.

Saroja S Bhusare et al, [7]: Proposes the BM of radix-8 with low error and fixed width that have 2 n-bit of inputs and produce n-bit of products. This conversion of 2n-bits into n-bits product is done by removing half the adder cells that are needed to feature the partial product. In further step error compensation biases are determined and given to inputs of the maintained adder cells so the truncation error will be minimum. By this technique, the numbers of PPs are reduced to n/3 and conjointly the quantity of adder cell id also reduced with compared to full width multiplier factor with a further overhead of one FA for comp. biasing. Simulation results shows big quantity of error reduction is achieved with this system.

Bahram Rashidi et al, [8]: Presented an implementation which is of low power and low cost booth-shift/add multiplier-based singed multiplier is presented. The most blocks of the circuit are created with some easy low-power structures. Here we use signed shifter and booth encoder based on multiplier, a Manchester adder based on multiplier, a management section, and for FA low power architecture is used. The proposed design is success synthesized and verified with Xilinx and Spartan-3 FPGA. The result shows by the power estimator shows that the power consumption of proposed methodology is very low.

Bipin et al, [9]: Explained typical changed Booth encoding which generates n/2+1 rows rather than n/2 rows and also irregular partial product (PP) array because of addition signed bit at the least significant bit (LSB) position of every row of PP. For generation of n/2 PP row along with array of regular partial product an approach is developed, which result reduction on power of MBE multipliers. Here for reducing the partial product rows to n/2 a technique of search out direct 2's complement has been also included with last PP row. Partial products have no change and regular as adding a LSB with negligible bit.

In addition with this for generation of final result different adders are taken and are compared. In final stage Ripple carry adder, CLA adder, and carry choose adder are used. We make an analysis that Carry choose adder shown improvement in delay parameter as comparison to hold look-ahead adder and ripple carry adder.

A. S. Prabhu et al, [10]: Showed an analysis that traditional multiplier is slow and consume more power in processor. So for reducing the ability consumption of multiplier, the Booth coding methodology is developed which provide low power system. This booth decoder can increase variety of zeros in number. Booth multiplier consists of decoder which converts input into equivalent to booth. As a result the shift activity will be reduced that the consumption of power. The input bit constant can verify the shift activity of the element that's once the input constant is zero that row or column is to be deactivate. Once number having a lot of zeros the overall power is minimum of design. Thus in BM maximum power reductions are done.

D. Jackuline Moni et al, [11]: Proposed multiplier for low power as well as high speed and can be arranged either for a single sixteen bit multiplication operation; it is a single multiplication of 8 bits or two parallel multiplications of 8 bits. The starting product can be shortened to an additional reduction in energy consumption and increase the speed by a little, the output process is sacrificed. Furthermore, the projected multiplier maintains a suitable output quality with enough accuracy once truncation is performed. In this approach the input is dynamically detect and turned off the operation of non-effective. Hence the unnecessary circuitry may be with efficiency deactivated, thereby power consumption is reduced and the speed of operation is increased.

IV. PROPOSED METHODOLOGY

For designing of higher bit multiplier we first require to design at lower scale, in our work we first design a multiplier for 2×2 design after designing and combining that we design 4×4 design and with the help of them the final required design of proposed 8×8 and 16×16 multiplier is to be designed.

Firstly we define the multiplier and multiplicand and on multiplier we first apply the modified booth formula as a result of this numbers of maximum 1's are reduced and many numbers of zero is to be generated. As numbers of 0's just require shifting operating and not require to calculate the partial product, hence numbers of Partial Products are to be minimized. After this the accumulation process is start for this Wallace scheme is to be used in which combination of CSA adder and CLA adders are used. As CSA is not fast adder but generates accurate result and CLA is fast adder because it consist Carry bypass logic. Hence average speed is maintained.

One of the most advanced types of design is proposed DSP application and for microprocessor. In this architecture accumulation is done with carry save adder (CSA) tree which reduce the numbers of PPs. In the proposed architecture, as we remove adder for addition operation the critical path is reduce and which result in the reduction in binary bits in the final adder. While this design is better in performance because of PP reduction and reduced critical path compared to the previous architectures, with the use FA the speed is decrease we must require to increase output rate of the final adder results for accumulation. In proposed technique we use N/3 bit of adder which increase the speed of operation. The basic multiplication processes that consist of four process module i.e. booth encoding, partial product summation, final addition and their accumulation. In booth encoding define the number of multiplicands bits and number of multiplier bits and then partial product has been done. The summation of these PP is to be done in very next process and then summation of these partial product has been done in process of final addition process and at the last result will store in the accumulator.

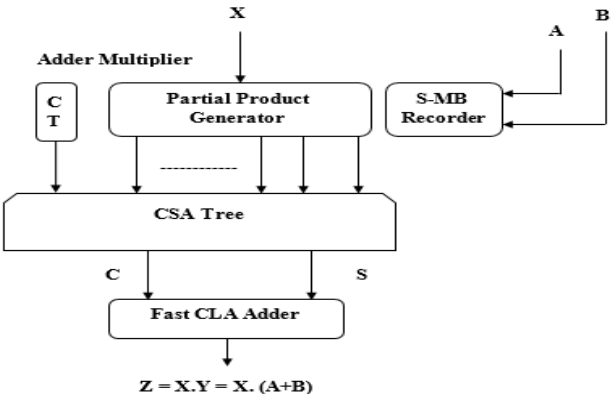

Figure 1: fused design with direct recoding of the sum of A and B in its MB representation

The PP generator generates seven candidates of the partial products, i.e., {-3A, -2A, -A, 0, A, 2A, 3A}. These are then selected according to the encoding results of the operand B. When the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree. Modified encoding is a prevalent form used in multiplication. It is a redundant signed-digit radix-8 Encoding technique. Its main advantage is that it reduces by half the number of partial products in multiplication as shown in Figure 1.

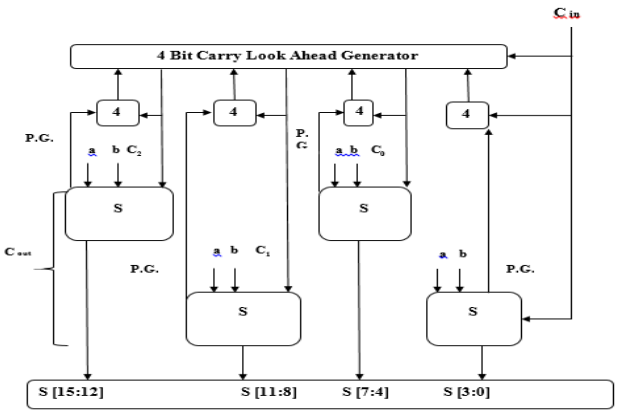

Figure 2: Hybrid CLA for 16 bits

The multiplier is a basic parallel multiplier based on the MB algorithm. The terms CT, CSA Tree and CLA Adder are referred to the Correction Term, the Carry-Save Adder Tree and the final Carry-Look-Ahead Adder of the multiplier. Carry Look Ahead Adder of the proposed mechanism shown in the figure 1.

In this section, we discuss the proposed method of hybrid carry look-ahead adder. This method is divided into three stages as like hierarchical carry look-ahead adder. The Figure 2 show the design of Hybrid CLA. In stage one, accept the two n-bit number of inputs and produce propagate and generator value. After finishing this stage, we move to next stage. In this stage we generate the intermediate carry and the overall carry is also generated. Now carry has to be generated from the top module because it occupy more space. One more advantage is that there is no need to generate the carry propagate (Pout) and carry generate (Gout) signals. Here the carry of the whole design is generated in the bottom stage of the structure. Simultaneously we can generate the sum of every bit. By this method the area of the design is reduced. So this is one way to design high speed and less area carry look-ahead adder design.

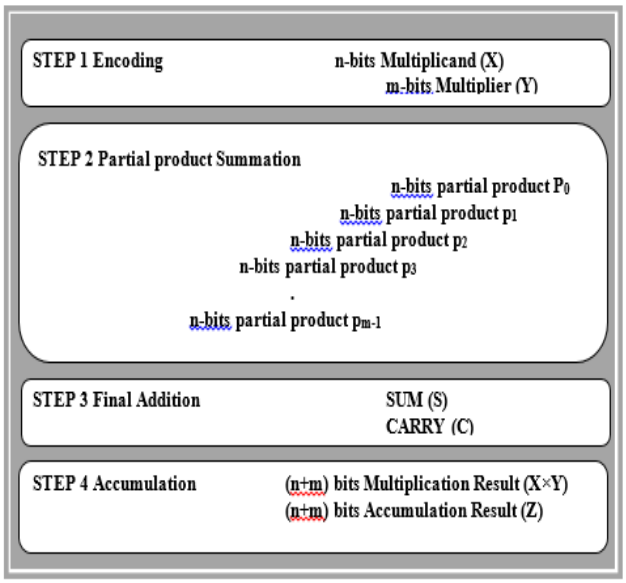

Figure 3: Proposed Circuit Design Flow

The figure 3 shows various steps of multiplication process in circuit.

Step 1: In first step booth encoding is done in which n-bits of multiplicand (X) and m-bits of multiplier (Y) are involved. Product has done in this process.

Step 2: This step shows process of summation of PP, in this process partial product summation has done by in shifting sequence.

Step 3: Process of final addition, in this process addition has done for all sequences which have generated through partial product summation process.

Step 4: Process of accumulation, in this process output final result after summing process is shown and store into the memory.

These steps of basic building block for multiplication circuit describe that the basic process multiplication.

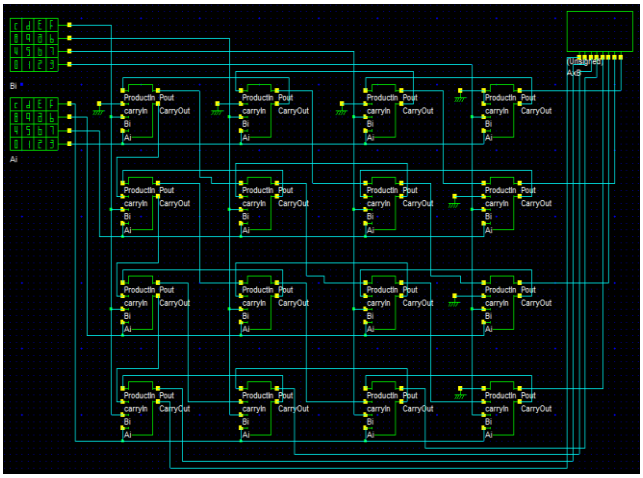

Figure 4: Proposed 16×16 Multiplier

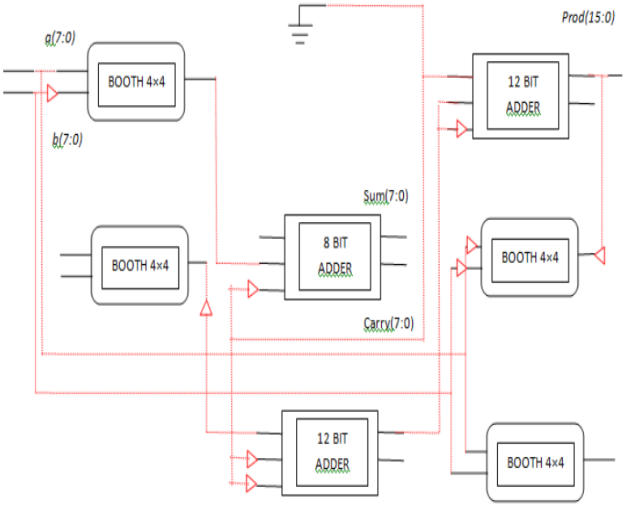

Figure 5: Proposed 8×8 Multiplier

The proposed architecture of Booth Multiplier 8×8 is shown in figure 5 which is the combination of 4×4 Booth Multiplier where the input is of 4-bit address namely two input a(7:0) and b(7:0) provide an output product of 16 bit (15:0).

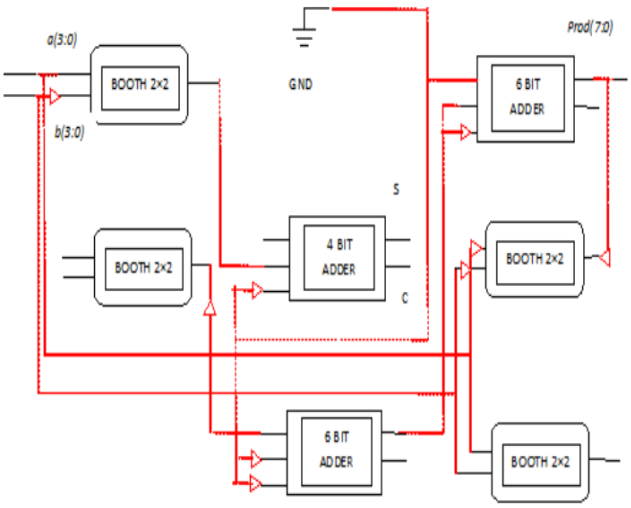

Figure 6: Proposed 4×4 Multiplier

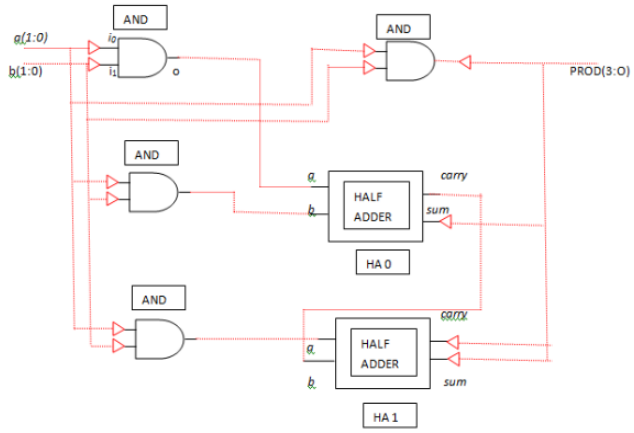

Figure 7: Proposed 2×2 Multiplier

For designing of 16×16 multiplier there are segments is to be divided firstly we design a 8×8 Booth multiplier which is combination of 4×4 booth multiplier. So for designing a higher radix system we implement firstly lower system after that with combining them with help of adder circuit we find our proposed circuit. The lines in the circuit are showing the connection of input output port and flow of current into the circuit.

V. SIMULATION RESULTS

In this paper we have proposed an efficient (low power consumption) Multiplier architecture employing two simulation software. Firstly, we use DSCH-2.7f for designing, Micro-wind 3.1a for layout and power analysis and behavior simulation and get the waveform of results.

1. DSCH Software Results

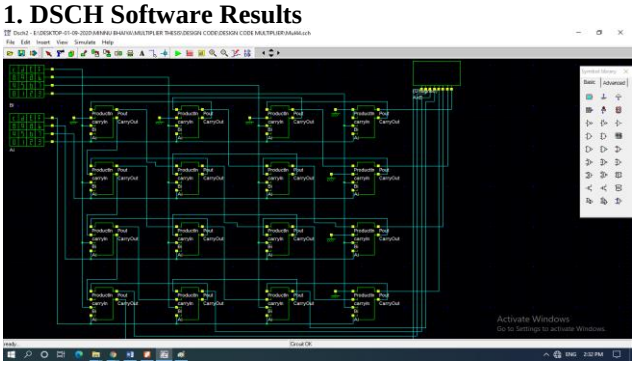

Figure 8: Proposed 16×16 Multiplier Circuit Module (32-bits)

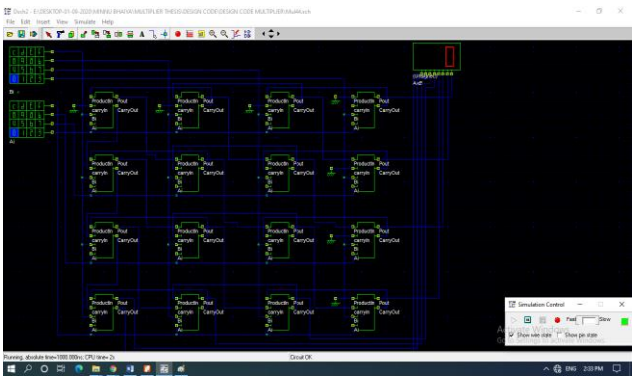

Figure 9: Simulation Results of Proposed 16×16 Multiplier Circuit Module (32-bits) when both input are A_i = "0" and B_i = "0"

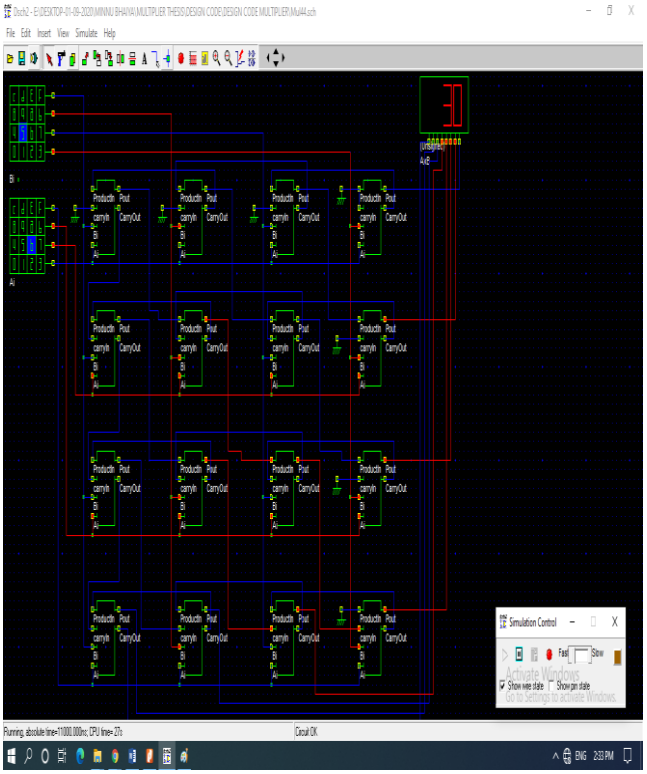

Figure 10: Simulation Results of Proposed 16×16 Multiplier Circuit Module (32-bits) when inputs are A_i = "6" and B_i = "5"

As above depicted figure 9 shows the simulation results of proposed 16×16 Multiplier Circuit Module (32-bits) when both inputs are $A_i = B_i$ = "0" and gets multiply results $A_i \times B_i$ = "0" at results blocks display. Similarly figure 10 shows that the simulation results of proposed 16×16 Multiplier Circuit Module (32-bits) when inputs are A_i = "6" and B_i = "5" respectively and gets results $A_i \times B_i$ = "30" at results block display.

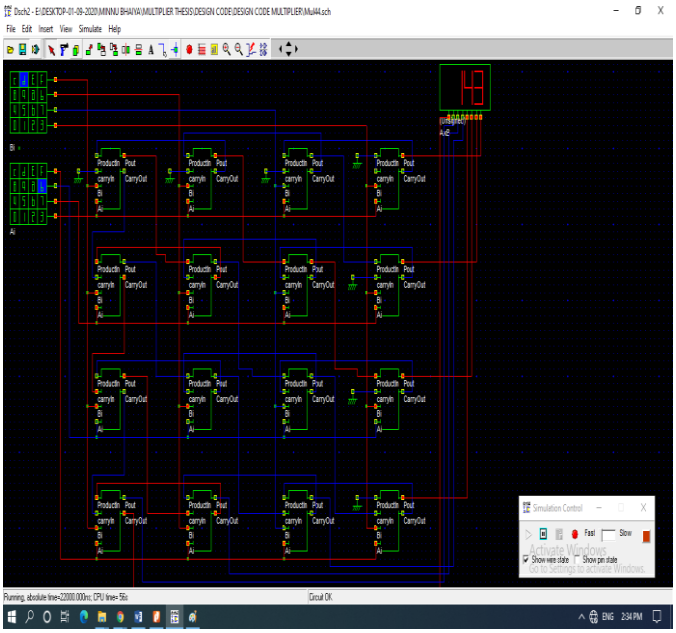

Figure 11: Simulation Results of Proposed 16×16 Multiplier Circuit Module (32-bits) when input are A_i = "b" = "11" and B_i = "d" = "13"

As above depicted similar figure 11 shows that the simulation results of proposed 16×16 Multiplier Circuit Module (32-bits) when inputs are A_i = "b" = "11" and B_i = "d" = "13" respectively and gets results $A_i \times B_i$ = "143" at results block display.

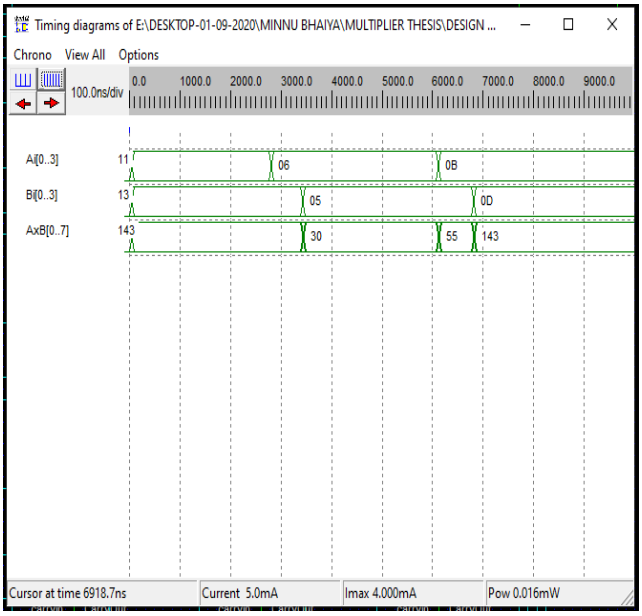

Figure 12: Timing Diagram of Proposed 16×16 Multiplier Circuit Module (32-bits) at Different Inputs

As above depicted figure 12 shows that the timing diagram of proposed 16×16 Multiplier Circuit Module (32-bits) at different inputs. An efficient in energy and low delay Multiplier has been designed with DSCH tool using Wallace Tree. The layout of energy efficient Multiplier has create on micro-wind tool at different nm technology like 180 nm and simulate with micro-wind. In this proposed work, we have design energy efficient Multiplier with advanced Wallace Tree concept. An adder cell using Wallace Tree plays a vital role in Multiplier architecture plan. The layout has made on micro-wind tool for fabrication and analysis of design methodology.

2. Micro-wind Software Results

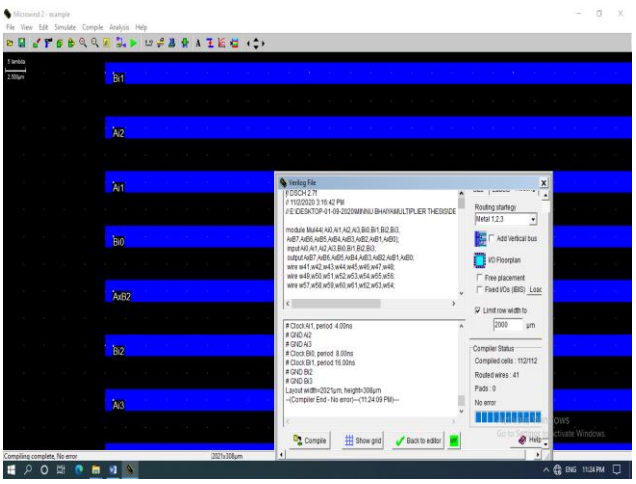

Figure 13: Compilation of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind for Layout Designing

As above depicted figure 13 shows that the Compilation of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind for Layout Designing and its shows no error and completed routed.

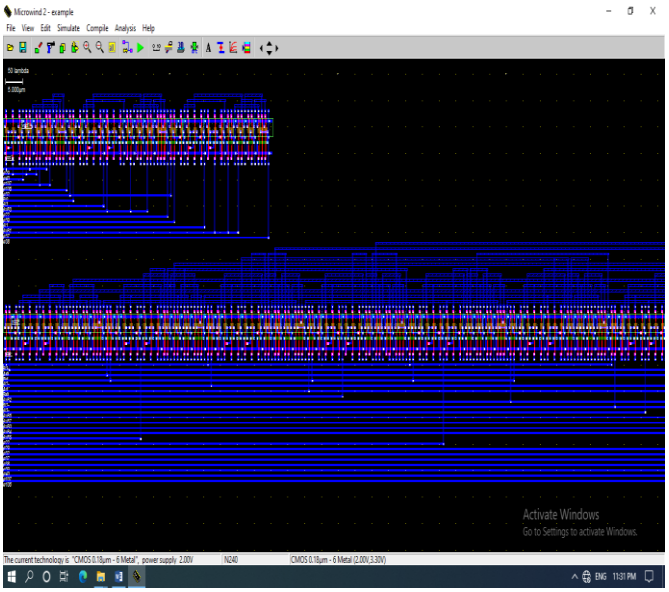

Figure 14: Layout of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind

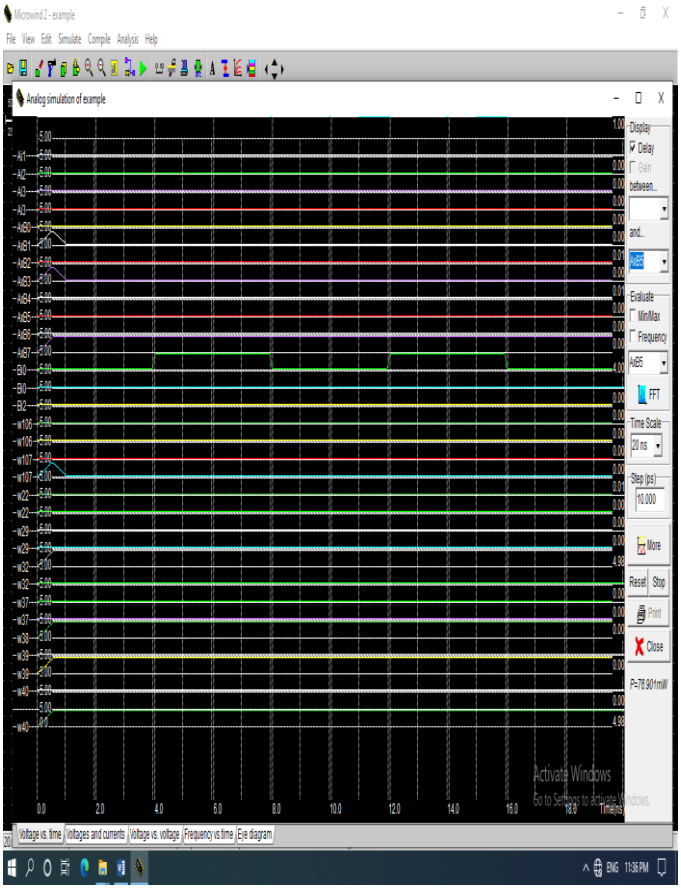

Figure 15: Power Analysis of Layout of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind

As above depicted figure 14 and 15 shows that the layout and power analysis of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind.

3. Comparative Power Consumption Analysis

Table 1: Comparison of Multiplier of Power Analysis

Word Size	Adder Type	Power
Modified 32_bit [1]	SQRT CSL	208 mW
Existing 32_bit [1]	RC adder	339 mW
Proposed 32_bit	Wallace Tree	**78.901 mW**

As above depicted table 1 shows the comparison of Multiplier in term of power consumption and its very clear form the table the proposed 16×16 proposed multiplier using Wallace tree concept shows less power consumption. The proposed multiplier shows 76.72% less power consumption as compare to existing multiplier using RC adder and also shows 62.06% less power consumption as modified multiplier using SQRT CSL adder cell.

VI. CONCLUSION

An efficient in energy Multiplier has been designed with DSCH tool using Wallace Tree. The layout of energy efficient Multiplier has create on micro-wind tool at different nm technology and simulate with micro-wind. In this proposed work, we have design energy efficient Multiplier with advanced Wallace Tree concept. An adder cell using Wallace Tree plays a vital role in Multiplier architecture plan. The layout has made on micro-wind tool for fabrication and analysis of design methodology.

The power analysis of Proposed 16×16 Multiplier Circuit Module (32-bits) in Micro-Wind presented following point.

The comparison of Multiplier in term of power consumption and its very clear form the table 5.1 the proposed 16×16 proposed multiplier using Wallace tree concept shows less power consumption. The proposed multiplier shows 76.72% less power consumption as compare to existing multiplier using RC adder and also shows 62.06% less power consumption as modified multiplier using SQRT CSL adder cell.

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