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Designing of Multiplier using different Adders: A Comprehensive Review

Mohini Yadav[1], Balram Yadav[2], Anshuj Jain[3]
[123]Dept. of Electronics & Communication Engineering, Scope College of Engineering, Bhopal, India
Mohiniy1402@gmail.com[1], balram.ieju@gmail.com[2]

Abstract- In modern world of technology we focus on ICs design with low power techniques and also on reduction of area of an IC. In digital circuits the multiplication is very common operation which mostly used in DSP applications and in microprocessors. As multiplier consumes some power and as well as require some area in memory so we must require a low-power, smaller area and higher speed multiplier design. In convention multiplier the process of multiplication is quite slow as it done in several stages like partial product generation and accumulation of these products as it take some time and also consume an amount of power. The Partial product reduction and fast addition can improve the system performance. At low radix the performance of system is better and power consumption of system is quite low but as we increase the radix the performance is poor as compare to lower one. This paper present a comprehensive review of multiplier design using different adder circuits.

Keywords: ICs, PP, CSA, CLA, RCA, Approximate Adder, Hybrid Adder Design.

I. INTRODUCTION

Every day integrated circuit technology gets additional advancement in style and performance. A faster style which consumes low power and smaller space is implied for trendy electronics styles. As advancement is done which help us to make proper utilization of energy, inscribe information and communicate info. From these technologies some of them techniques provide low power consumption design which are useful in several of applications [2-3]. In many of applications, digits and numbers are basically used for calculation, as in multiplier it is quite essential for calculation. Multipliers usually basic component in circuits which takes large space and consume a quality of power. Thence low power number multiplying design style is demanding in VLSI system style [1] [6]. New techniques are developing to make low power multipliers on technological advances, physical, circuits and logical levels. As the bit is slow processing element in digital circuit, the output of system can be determined by partial products which also define system performance, addition in the multipliers are important element in a style itself [4-5]. Therefore, optimizing the speed and space of any number is difficult task now a day. However, the space and speed range of the unit sometimes conflicting constraints as the speed increase which results in increment in Area. As circuit area and power consumption are linearly related to each other so we must make compromise between them, as speed of the system for a bigger improvement in reduction of power and space.

This section of paper discuss the introduction about the topic and rest of the paper describe as follows, section II discusses the multiplier design, and review of literature present in the section III, section IV discusses the problem statement and conclusion of the paper discusses in the section V.

II. MULTIPLIER DESIGN

Multiplication process is done in following basic steps: firstly partial products are generated (PPG), then partial product reduction (PPR) and possibly at the top adding Carry propagate (CPA). Normally, we have combined and provide numbers for implementations ordered. As we have a tendency to surface unity that penetrates into the combinable case only in the mind, since the dimensions of integration are currently cultivated enough to begin with accommodating parallel number applications in circuits [7-8]. Every multiplication algorithms have different technique for multiplication process which include PPG, PPR and addition, The algorithm is for reduction of partial products and also for reduction of area as well as delay, from them one operand is to be recorded on high radix set.

We make an analysis on higher radix which has a set of digits given for PPG and for PPR, two methodologies are implemented, one of them is row based reduction which is done by considering an adder, another is column based reduction which can be done by considering a counter array. In execution the process addition requires a fast adder arrangement for quick result because it is on the critical path. In some times the final addition result is vary when we keep redundant results from partial products into consideration for further arithmetic operations.

III. REVIEW OF LITERATURE

Here we discuss methodologies that are similar to our works and provide solution for minimizing the power optimization of circuit. Here power and system performance of different techniques are compared. The key's to show energy and delay tradeoff for several totally various optimizing techniques together. In microprocessors and digital process implementations we require the computation of number operation. Specifically, speed, space and low power multiplication implementation

is a difficult task. Some existing techniques are available which minimize the dynamic power of circuit.

In general, there are serial and combinable number implementations. In this, multiplication process includes three steps are done namely PPG, PPR and at last step carry propagate addition. In this work a combined technique is used and as a result of the dimensions of integration now's we must accept that multiple techniques are taken into consideration for digital VLSI systems.

Nandan K. S. et al. [1]: Throughout this study introduced a 4:2 compressor, capable of integrating accurate and estimated operating modes, this compressor gave the operating modes is of faster speed and decreased power reliability. These compressors are aimed to include a multiplier that significantly enhances the reliability (as well as power and speed) of a 32-bit Dadda multiplier throughout operation. The structure criteria were substantially better when comparing and compressor related inexact multiplier.

This paper presents a clear approach to reducing CSL adder architecture area, delays and power. The typical CSL adder have drawback of high power usage and more chip areas. A small power, smaller delay and minimized area have become available for the changed SQRT CSL adder using CB logic than any other adder structure. New technologies can be designed to reduce power usage. Additional constraints may be optimized such as size, gate clock number, width and more. The results are evaluated for such constraints as area, delay and power. These are the essential constraints.

K. Tsoumanis et al, [2]: Proposes pre encoded radix-4 multiplier based on on-off encoding with extend to non-redundant radix-4 signed digit(NR4SD) encoding. NR4SD algorithm provides better results as compare to conventional BM .With NR4SD technique the numbers of generated partial products are decrease and hence the system operation performance is increased and power consumption of circuit is reduced.

Balakumaran R et al, [3]: Proposed a method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid CLA adder. MB algorithm provide less delay and low power multiplier as compare to conventional Booth and it also reduce the numbers of PP. Here CLA adder is introduce for maintaining the MAC delay. The reversible logic is used for reduction of complexity of circuit, minimizing power consumption of circuit and loss of knowledge. Here we make a survey on doable ways in which to form a FA style using completely different reversible logic gates.

Liangyu Qian et al, [4]: Presented approximate or inexact computing has better result and suitable for various applications because of its potential benefits with relation to low power consumption and high performance.

They present the planning of associate approximate number; this approximate multiplier consists of an approximate Booth encoder, an approximate 4-2 compressor and an approximate tree structure. The proposed approach also implemented for 8-bit, 16-bit and also applicable for 32-bit signed multiplication schemes with focusing on embedded systems applications. Simulation results compared with a particular Wallace-Booth number also as different approximate multipliers found within the technical literature, the planned approximate theme achieves important enhancements in area, delay, power consumption, and combined metrics.

Kiamal Pekmestzi et al, [5]: Presented an approach with 2's complement representation, this representation widely used as compared to other, signed number systems provide an advantage of single representation of zero as well as simple addition. Signed magnitude is used in signaling applications for representing the signal for low power analysis. Also 1's compliment is better for representation as it is easy to make conversion between signed magnitude and them. Therefore, for this system we should analysis various efficient arithmetic design. In this proposed work 1's complement Booth multiplier is proposed which having similar complexity level as of 2's complement.

Honglan Jiang et al, [6]: This paper explained PP reduction issue resolved by approximate style. Here approximate 2-bit adder is designed. After that with help of 2-bit adder we implement a short section for coding which results in triple number generation and carry propagation is not occurs.

With a compromise between power consumption and accuracy, during this work, totally different signed 16×16 bit approximate radix-8 BM styles are planned. In this design all the limitations and problems of radix-8 is to be solve. In this approximate design of radix-8 the architecture consist of ABM1 and ABM2, here we use truncation technique which helps us in reduction of time and power of system. The data processing with help of Wallace tree is then taken into consideration for fast addition of PP, which results speed of operation is increased.

Saroja S Bhusare et al, [7]: Proposes the BM of radix-8 with low error and fixed width that have 2 n-bit of inputs and produce n-bit of products. This conversion of 2n-bits into n-bits product is done by removing half the adder cells that are needed to feature the partial product.

In further step error compensation biases are determined and given to inputs of the maintained adder cells so the truncation error will be minimum. By this technique, the numbers of PPs are reduced to n/3 and conjointly the quantity of adder cell id also reduced with compared to full width multiplier factor with a further overhead of one FA for comp. biasing. Simulation results shows big quantity of error reduction is achieved with this system.

Bahram Rashidi et al, [8]: Presented an implementation which is of low power and low cost booth-shift/add multiplier-based singed multiplier is presented. The most blocks of the circuit are created with some easy low-

power structures. Here we use signed shifter and booth encoder based on multiplier, a Manchester adder based on multiplier, a management section, and for FA low power architecture is used.

The proposed design is success synthesized and verified with Xilinx and Spartan-3 FPGA. The result shows by the power estimator shows that the power consumption of proposed methodology is very low.

Bipin et al, [9]: Explained typical changed Booth encoding which generates n/2+1 rows rather than n/2 rows and also irregular partial product (PP) array because of addition signed bit at the least significant bit (LSB) position of every row of PP. For generation of n/2 PP row along with array of regular partial product an approach is developed, which result reduction on power of MBE multipliers. Here for reducing the partial product rows to n/2 a technique of search out direct 2's complement has been also included with last PP row. Partial products have no change and regular as adding a LSB with negligible bit.

In addition with this for generation of final result different adders are taken and are compared. In final stage Ripple carry adder, CLA adder, and carry choose adder are used. We make an analysis that Carry choose adder shown improvement in delay parameter as comparison to hold look-ahead adder and ripple carry adder.

A. S. Prabhu et al, [10]: Showed an analysis that traditional multiplier is slow and consume more power in processor. So for reducing the ability consumption of multiplier, the Booth coding methodology is developed which provide low power system. This booth decoder can increase variety of zeros in number. Booth multiplier consists of decoder which converts input into equivalent to booth. As a result the shift activity will be reduced that the consumption of power. The input bit constant can verify the shift activity of the element that's once the input constant is zero that row or column is to be deactivate. Once number having a lot of zeros the overall power is minimum of design. Thus in BM maximum power reductions are done.

D. Jackuline Moni et al, [11]: Proposed multiplier for low power as well as high speed and can be arranged either for a single sixteen bit multiplication operation; it is a single multiplication of 8 bits or two parallel multiplications of 8 bits. The starting product can be shortened to an additional reduction in energy consumption and increase the speed by a little, the output process is sacrificed.

Furthermore, the projected multiplier maintains a suitable output quality with enough accuracy once truncation is performed. In this approach the input is dynamically detect and turned off the operation of non-effective. Hence the unnecessary circuitry may be with efficiency deactivated, thereby power consumption is reduced and the speed of operation is increased.

TABLE 2.1: Table of review on different methods and their contribution

S. No.	Approach Used	Author	Year	Publisher	Contribution
1	NR4SD	K. Tsoumanis	2016	IEEE	Off-line encoding of coefficient uses the (-1, 0, +1, +2)
2	Hybrid CLA	Balakumaran R.	2017	ICCPCT	Proposed a hybrid CLA and reversible logic for reduction of circuit complexity
3	Approximate high bit design with truncation technique	Honglan Jiang	2016	IEEE	Truncation technique is to reduce power and execution time
4	Minimize the number of adder cell and truncation error	Saroja S Bhusare	2016	IEEE	Used Wallace tree method and minimize the number of cell as result number of PP reduces
5	Low power multiplier	S.Prabhu	2012	IEEE	Numbers of one is reduced by algorithm hence less numbers of partial products are generated.

IV. PROBLEM STATEMENT

To implement or style the efficient multiplier from this literature survey we face some drawback and additionally their some limitation of typical sort booth multiplier. Currently to style or implement the projected methodology of energy efficient and high performance booth multiplier face some drawback that is present within the previous typical type booth multiplier.

1) Design space and power of multiplier should be a lot of which are often scale back by the projected technique of designing.

2) Recoding of total sum directly which was not present within the previous design of multiplier style.

3) A typical booth multiplier cannot reduce the partial product however it may well be reduce by the projected technique of designing.

4) In existing state of design it is quite difficult and challenging task to design quick response and low power consumption BM because as we increase numbers of bits in multiplication the numbers of PP is increase which increase the memory size and also reduce the performance of system.

V. CONCLUSION

After going through all the literature survey and review of past work and after facing a lot of problems in previous base work, we are able determine the objectives of the research work that are to implement multiplier encoding Algorithm for the design of a binary multiplier using different architectures and power analysis at various levels. To study the space and also the time delay that consumed by distinct adders and located out an optimum relationship among the time and space complexity the adders which we have there into consideration? After examining all it might be finalized that no of bits changes are best fitted for Low Power Applications. Then the research turned focus toward the area and delay of Multipliers. Further work can be done on design a higher bit multiplier and estimated its delay, area.

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