International Journal of Engineering Technology and Applied Science

(ISSN: 2395 3853), Vol. 4 Issue 3 March 2017

# A CMOS Full Adder Design for low power applications Using Hybrid Logic

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***Abstract-*** In this paper the architecture designs speed and area efficient transistor base adder using static CMOS pass transistor logic. In this work the longest critical path shortened to decrease the total critical path delay. The propose design is high speed and less number of transistor architecture. For this a Complementary Metal Oxide Semiconductor (CMOS) Transmission Gate (TG)-based adder block has been designed. This block is designed to be connected to other 4 bits blocks to form higher bit adders. The proposed design circuit has been use for the implementation of 8, 16, 32 and 64 bits adders using transmission gate base logic and the timing simulation of its layout results verified its efficiency. This work shows that for low power applications in 50nm technology. The propose CMOS layout of 8 bit adder with carry select logic is design on MICROWIND Layout Simulator tool. In this the three four bit ripple carry adder is design with five 2X1 multiplexer. Channel length of MOSFET is 0.05 µm and that channel width is 0.125 µm. The area of design is 158 $\mu m^2$. The power dissipation of design is 1.941uW. The design of 8 Bit Adder using Propose Carry Bypass Logic has 342 transistors comprises of 171 NMOS and 171 PMOS transistor.

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**KEYWORDS: Energy Efficient Design, FA, CMOS, Carry By-Pass Logic, Complexity, Area.**

## I INTRODUCTION

Day by day IC technology is obtaining a lot of advanced in terms of style and its performance analysis. A faster style with lower power consumption and smaller space is implicit to the trendy electronic styles. Full adder usually have extended latency, large space and consume substantial quantity of power. Thence low-power full adder style has become a very important part in VLSI system style. Everyday new approaches are being developed to style low-power full adder at technological, physical, circuit and logic levels. Since the full adder is mostly the slowest part during a system, the system's performance is set by performance of the multiplier. Conjointly full adder designs are the foremost space overwhelming entity during a style. Therefore, optimizing speed and space of a full adder may be a major style issue today. However, space and speed are typically conflicting constraints in order that rising speed leads to larger areas and vice-versa. Conjointly space and power consumption of a circuit are linearly related to. Thus a compromise has got to be exhausted speed of the circuit for a bigger improvement in reduction of space and power.

A higher illustration base effectively indicates to fewer digits. Embedded systems style focuses on low Power dissipation and system-on-chip. A reliable on-chip communication customary is a must in any SOC. This section provides an informative review regarding the designing existing mechanism of full adder combinational circuit.

Energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e. electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e. magnetic field energy, into the digital circuit. If one relates the signal change to the conversion of electric energy to magnetic energy the so-called "energy-recovery" can be realized. This is the method by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e. resistors, is largely reduced or avoided. The energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic and various domino logics. However, those circuits still rely on DC power, and the energy conversion remains as electric energy to heat. There is need for further study in the case of circuits supplied with AC power. The AC power controls the working rhythm of the circuit and acts as the clock, called the power-clock.

The research shows that the adopted power clock with gradually changing process during its rising and falling dissipates only less energy for charging and discharging the node capacitance through the conducting of MOS transistor. The "adiabatic" switching operation is resulted, by which a new approach to design low power CMOS circuits is proposed. Clocked CMOS circuits with gradually rising and falling power-clock were expected to obtain a significant energy saving. It attracts many researchers to study this issue in recent years. However, the operational constraint that the output signal should track the power clock's gradually rising and falling behavior to accomplish the charging and discharging process increases

the difficulty in the circuit design. At present, the existing research either adopts retractile cascade power clock or adopts multiple phase power clock with memory schemes.

The new research on the energy recovery CMOS circuit should start from its basic theory, including the basic algebraic expressions and the basic properties of clocked signals. At the same time, both the basic clocked CMOS gate and the clocked flip-flop, the basic unit of energy recovery CMOS circuits, should be investigated at the beginning. With the above view this research will focus on these two topics.

A variety of full adders using static and dynamic logic styles has been reported in literature, 34 of which have been stated by (Jiang et al 2008) alone, including the most well-known static complementary CMOS adders using 28 transistors and 40 transistors.

## II LITERATURE SURVEY

The research [1] introduce that the full adder cells play a vital role in numerous VLSI circuits. Therefore, design of an energy-efficient full adder which operates reliably in submicron technologies has become a great concern in recent years. Some previously designed cells suffer from non-full swing outputs, high-power consumption and low speed issues. In this paper, two high-speed, low-power and full swing full adder circuits are designed in 90-nm CMOS technology. According to simulation results, the proposed circuits have rail to rail output signals. Also, an improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay, power consumption and power-delay product (PDP), respectively.

In this paper [2], hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve Low power and high speed. Hybrid logic style used is the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The Circuit was implemented using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA) and Transmission Function adder (TFA). Average Power consumption of the proposed design is found to be 1.114 μW at 90nm for 1.2V supply and 5.641 μW at 180nm for 1.8Vsupply. Delay in the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies respectively. Thus consuming extremely low power and requires less time than existing designs for the same testing environment. Power Delay Product (PDP) is calculated as product of Power and delay values signifies energy requirement of the design. Proposed design requires 71% less energy than TFA and 81% less energy than TGA and 92% less energy than conventional CMOS adder.

The research article [3] proposed that the designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is array multiplier. Array multiplier half adder have been used to sum the carry products in reduced time. Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier, which is the major power consuming element in the digital circuits. Basically the process of multiplication is realized in hardware in terms of shift and add operation. The optimization of adder has led to the improvement in performance of multiplier. In this paper, a modified full adder using multiplexer is proposed to achieve low power consumption of multiplier. To analyze the efficiency of proposed design, the conventional array multiplier structure is used. The designs are developed using Verilog HDL and the functionalities are verified through simulation using Xilinx. The ASIC synthesis results of the proposed multiplier shows an average reduction of 35.45% in power consumption, 40.75% in area, and 15.65% in delay compared to the existing approaches.

In modern nanotechnology and quantum computation [4], reversible logic plays a pivotal role as it has minimal impact on physical entropy. Reversible logic gates have same number of input and output hence power loss due to bit erase operation can be avoided. There are many reversible logic structures which can perform different Arithmetic and logic operations as traditional or classical logic structures can do. In this paper, two reversible logic structures are proposed which can perform operation of addition. These logic structures namely proposed design I and Proposed design II, generate carry output signal and carry propagate signal on the basis of two reversible logic gates known as Fredkin gate and Feynman gate. Performance of proposed designs is evaluated in terms of quantum cost, constant input, garbage output and delay. It is found that proposed design II is a better choice over proposed design I and some other existing Designs.

The Paper [5] discussed the comparative analysis of different Fin-FET based full adder cells designed with various logic styles. The logic styles used for implementation of Fin-FET based 1-bit full adder are Complementary MOS (CMOS), Transmission Gate (TG) and Complementary Pass-Transistor Logic (CPL). The simulations have being done at 10nm, 20nm and 32nm technology node for all full adder cell designs. PTM models for multi-gate transistors (PTM-MG) low power are used for simulations. The performance parameters that were measured, analyzed and compared are average power, leakage power, delay, and energy. It is observed that less power is consumed in Transmission Gate (TG) based full adder than the Convention full adder and complementary pass-transistor logic (CPL) based full adder in 10nm

technology node. Also, found reduction in delay, EDP, and PDP in TG based full adder compared to other cell designs.

The paper [6] very large-scale integrated circuit (VLSI) design, based on today's CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of non-volatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. They also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full non-volatility for future nonvolatile microprocessors.

The research [7] introduce the solution of the serious problem of threshold loss that causes non-full-swing at the out-put of 1-bit full adder, an arrangement in which all the transistors are forced to operate in sub-threshold regime is proposed in this paper. But this will in turn bring additional area and delay overhead. In this work, full swing at the output of 1-bit full adder is retained with reduced area and delay overhead. An additional capacitor working in the differential voltage mode will be replacing the transistor that is used to reduce the threshold loss problem at the output of 9T based full adder as discussed in this paper. Previous works related to this domain concerns about reduction of power of only 1-bit adder. The work targets power and area reduction of 1/4/8/16 bit adders. Proposed adder shows maximum total power saving of 46.87 % and 25.99 % with respect to 8T and 9T adder configurations respectively.

This paper [8] present, a three transistor XNOR gate. The proposed XNOR gate is designed using CADENCE EDA tool and simulate using the SPECTRE VIRTUOSO at 180 nm technology. The proposed results are compared with the previous existing designs in term of power and delay. It is observed that the power consumption is reduced by 65.19% for three transistor XNOR gate and 48.11% for eight transistor full adder. It is also observed that the delay is reduced by 31.82% for three transistor XNOR gate and 28.76% for eight transistor full adder.

This paper [9] proposes the design of a low power, high speed, and energy efficient full adder using modified Gate Diffusion Input (GDI) and Mixed Threshold Voltage (MVT) scheme in 45nm technology. The proposed design on comparison with the traditional full adder composed of CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), respectively, exhibited a considerable amount of reduction in terms of average power consumption (Pavg), peak power consumption (Ppeak), delay time, power delay product (PDP), energy delay product (EDP) as well as transistor count and hence surface area. Pavg is as low as 7.61x10-7 watt while Ppeak is as low as 6.21x10-5 watt, delay time is found to be 2.05nano second while PDP is computed to be as low as 1.56x10-15 Joule and EDP is evaluated to be as low as 3.20x10-24 Js for 0.9 volt power supply. The simulation of the proposed design has been performed in HSPICE and the layout has been designed in Micro-wind.

In this paper [10] they have designed the full Adder using hybrid-CMOS logic style by dividing it in three modules so that it can be optimized at various levels. First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. It also consumes minimum power and provides better delay performance. Second module is a sum circuit which is also a XOR circuit and uses carry input and the output of the first module as input to generate sum output. Third module is a carry circuit which uses the output of the first stage and other inputs to generate carry output. In the new full adder design we have proposed new full adder circuit which reduce the power consumption, delay between carry out to carry in and PDP by 12 to 100%. Simulations are carried out on HSPICE using TSMC 0.18 μm CMOS technology.

## III PROBLEM STATEMENT

Performance factors such as power, delay, and layout area were evaluated with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS output drive full adder. Due to toughness beside CMOS scaling and transistor sizing with the overhead of high input capacitance and requirement of buffers, the adder using this static CMOS. Also this design proves the power dissipation cause due to the stray capacitances and large length interconnects. The circuits design using CMOS logic with large number of transistors and maximum length interconnect are gradually more existing provider to propagation delay, overall area and power consumption. The main goal of this work is to improve the different function parameters such as power dissipation, path propagation delay and number of transistor used in full adder design compared with the previously existing ones.

Floating point (F.P.) addition is a preferable operation for a wide range of applications. The main areas in which they work are area-efficient, dynamically configurable, multi precision architecture for F.P. addition. In our work the use of transmission gate decreases the number of transistors which overcomes the area tradeoffs. The main

drawback of the parallel adder is that the delay rises linearly with the bit length. Hence planned design will have:

- How circuit components get integrate?
- How to design and implement Dynamic CMOS gates and a set of experiments and results considering the features of the implemented gates.
- Representation of wiring connectivity in adder circuit.
- Presentation of every gate level property like truth table.
- Representation of connectivity of gates.
- For floating point numbers we design a power and area efficient adder.
- To overcome slow speed of a parallel adder and propagation delay of the carry.
- The main drawback of the parallel adder is that the delay rose linearly with the bit length.

## IV PROPOSED METHODOLOGY

A half-adder is an arithmetic block which is used to add two bits. Such a circuit thus has two inputs which represent the two bits are to be added with which we get two outputs, with one generating the SUM output and the other generating the CARRY. Table 1 shows the truth table of a half-adder, showing all possible input combinations and the corresponding outputs. The Boolean expressions for the SUM and CARRY outputs are given by the equations are expressed below:

$$SUM = A\bar{B} + \bar{A}B$$

$$CARRY = A.B$$

**Table 1: Truth Table of Half Adder**

| A | B | SUM | CARRY |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

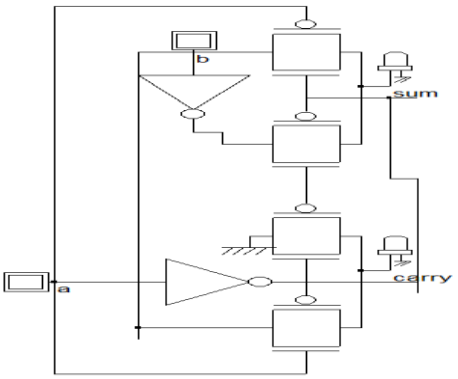


**Figure 1: Transmission Gate Base Half-Adder**

An examination of the two expressions informs that there is no scope for further simplification. While the first one representing the SUM output from an EX-OR gate, the second one representing the CARRY output from an AND gate. However, these two expressions can definitely be represented in different forms by using various laws and theorems of Boolean algebra to demonstrate the flexibility that the designer has simple a combinational function in hardware-implementing as of a half-adder.

**Transmission Gate Base Full Adder:** A full adder circuit is an arithmetic circuit block which is used to add three bits to generate a SUM and a CARRY output. Such a building block becomes a requirement when it comes to adding binary numbers with a large number of bits. The full adder circuit is used to overcome the limitation of the half-adder, which can be used to add two bits only. Let us recall the process for adding larger binary numbers. We start with the addition of LSBs of the two numbers. We save the sum in the LSB column and if any carry comes then we will forward it to the higher column bits. As a result, when we add the next adjacent higher column bits, we have a requirement of three bits if there were a carry from the previous addition. We have a same situation for the other higher column bits also, until we reach the MSB. We use full adder for the hardware implementation of an adder circuit which is capable of adding larger binary numbers but a half-adder is used for addition of LSBs only.

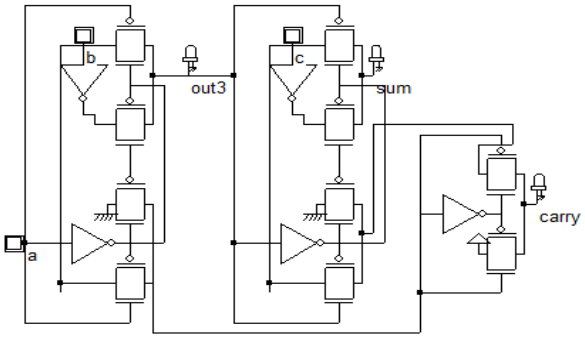


**Figure 2: Transmission Gate Base Full Adder**

The above diagram of full adder describes the basic building block of binary adders. However, a single full adder circuit is used to add one-bit binary numbers only. A cascade arrangement of these adders can be used to construct adders which are capable of adding binary numbers with a larger number of bits.

## V LAYOUT DESIGN & SIMULATION

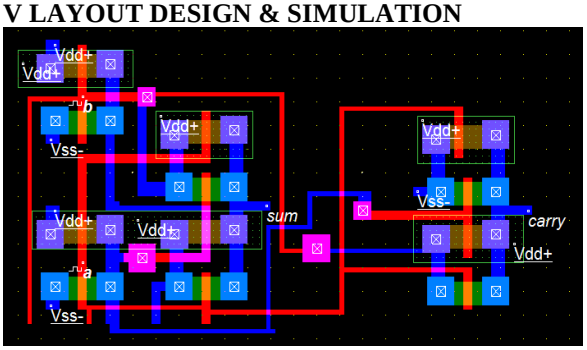


**Figure 3: CMOS Layout for Half Adder logic**

Figure 3 shows the CMOS Layout for Half Adder logic designs using transmission gate with six NMOS and six PMOS transistors. The channel Length of transistor is 0.05µm and its channel width is 0.125µm. The channel length area of TG logic is 0.6µm and that of overall area is 0.9µm2. The average power dissipation of TG circuit is 0.15µW with the switching delay of 0.001nsec to 0.05ns.

**Table 2: Configuration of Half Adder CMOS Logic**

| A | B | Sum | Carry | No. of T | O/P Load | Power Dissipation | Delay |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 12 | 0.42Ff | 0.15Uw | 0.001 ns to 0.05 ns |
| 0 | 1 | 1 | 0 | | | | |
| 1 | 0 | 1 | 0 | | | | |
| 1 | 1 | 0 | 1 | | | | |

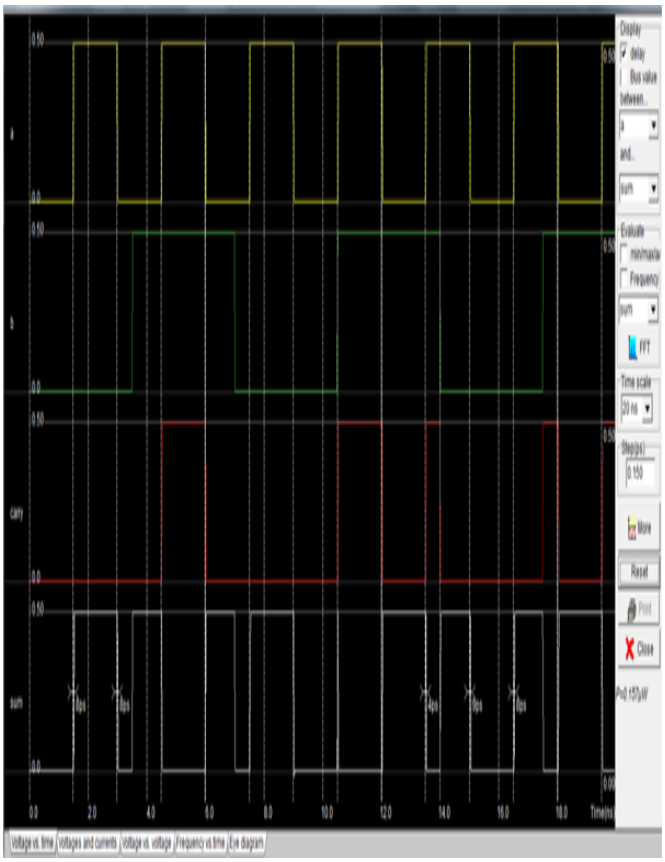

**Figure 4: Timing Simulation for Half Adder logic**

The timing simulation of half adder logic using CMOS logic is shown on 20ns timing scale. For the input a, b = 00 the sum and carry output is 00, for the input a, b = 01 the sum and carry output is 10, for the input a, b = 10 the sum and carry output is 10 and for the input a, b = 11 the sum and carry output is 01.

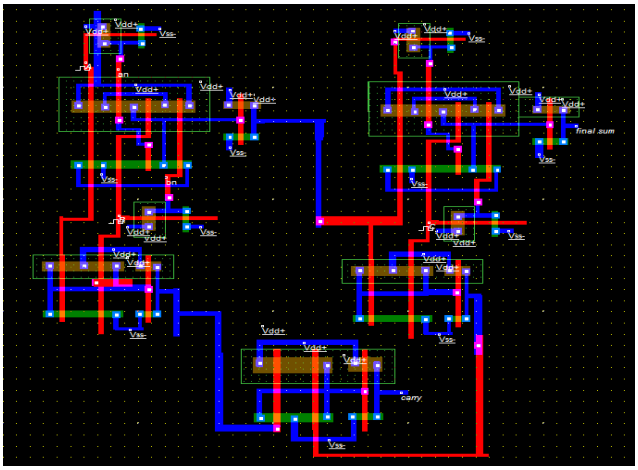

**Figure 5: CMOS layout for Full Adder CMOS Logic**

Figure 5 shows CMOS layout for full adder logic in which we are providing three inputs and get two outputs and this full adder design are using CMOS logic includes 23 NMOS and 23 PMOS transistors.

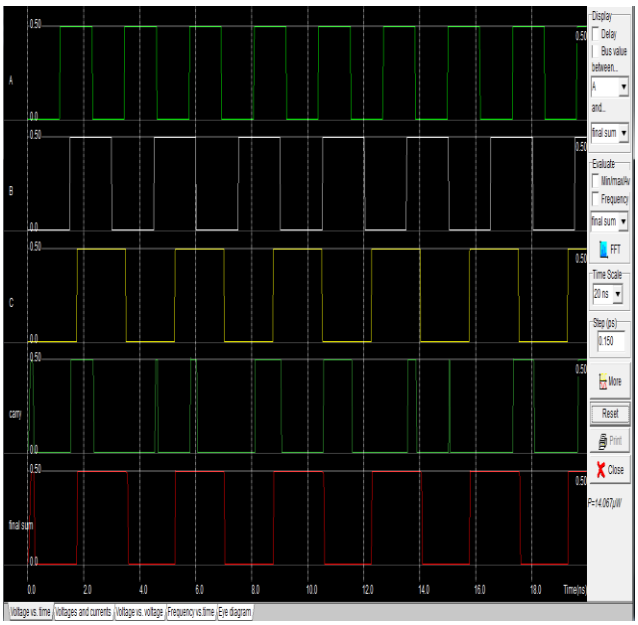

**Figure 6: Timing Simulation of Full Adder CMOS Logic**

The timing simulation of half adder logic using CMOS logic is shown on 20ns timing scale. For the input a, b = 000 the sum and carry output is 000, for the input a, b = 001 the sum and carry output is 10, for the input a, b = 100 the sum and carry output is 10 and for the input a, b = 111 the sum and carry output is 11.

**Table 3: Configuration of Full Adder CMOS Logic**

| A | B | C | Sum | Carry | No. of Transistor | Output Load | Power Dissipation | Delay (Tr/Tf) | Area |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 26 | 0.32fF | 0.331uW | 0.005/0.001ns | $13um^2$ |
| 0 | 0 | 1 | 1 | 0 | | | | | |
| 0 | 1 | 0 | 1 | 0 | | | | | |
| 0 | 1 | 1 | 0 | 1 | | | | | |
| 1 | 0 | 0 | 1 | 0 | | | | | |
| 1 | 0 | 1 | 0 | 1 | | | | | |
| 1 | 1 | 0 | 0 | 1 | | | | | |
| 1 | 1 | 1 | 1 | 1 | | | | | |

## VI CONCLUSION

The propose design is high speed and less number of transistor architecture of adder design. For this a CMOS Transmission Gate (TG) based adder block has been designed. This block is designed to be connected to other 4 bits blocks to form higher bit adders. The CMOS layout of transmission gate base 32 bits carry chain consist of 32 transmission gates base AND gate and OR gates. The total number of transistors require for design of 32 bits carry chain is 192 NMOS and 192 PMOS transistors. For the channel length of 0.05µm and channel width of 0.125µm the total area is calculated as 921.6µm2.

The CMOS layout of transmission gate base 64 bit carry chain consist of 64 transmission gate base AND gate and OR gates. The total number of transistors require for design of 64 bits carry chain is 384 NMOS and 384 PMOS transistors. For the channel length of 0.05µm and channel width of 0.125µm the total area is calculated as 3686.4µm2 The propose CMOS layout of 8 bits adder with carry select logic optimizes the speed, power and area. The three four bit ripple carry adder is design with five 2X1 multiplexer. Channel length of MOSFET is 0.05um and that f channel width is 0.125µm. The area of design is 158 µm2. The power dissipation of design is 1.941µW. The design of 8 bits Adder using Propose Carry Bypass Logic have 342 transistors comprises of 171 NMOS and 171 PMOS transistor.

## REFERENCES

[1] Majid Amini Valashani and Sattar Mirzakuchaki, "Two New Energy-Efficient Full Adder designs", 24th Iranian Conference on Electrical Engineering (ICEE) IEEE 2016.

[2] M Nikhil Theja and Dr T Balakumaran, "Energy Efficient Low Power High Speed Full adder design using Hybrid Logic", International Conference on Circuit, Power and Computing Technologies [ICCPCT] IEEE 2016.

[3] S. Srikanth and I. Thahira Banu et al., "Low Power Array Multiplier Using Modified Full Adder", 2nd IEEE International Conference on Engineering and Technology (ICETECH), Coimbatore, TN, India, 17th & 18th March 2016.

[4] Varun Pratap Singh and manish rai, "Verilog Design of Full Adder Based on Reversible Gates", IEEE 2016.

[5] Shivani Sharma and Gaurav Soni, "Comparison Analysis of FINFET Based 1-Bit Full Adder Cell Implemented Using Different Logic Styles at 10, 22 and 32nm", IEEE 2016.

[6] Ramin Rajaei and Sina Bakhtavari Mamaghani, "Ultra-Low Power, Highly Reliable, and Nonvolatile Hybrid MTJ/CMOS Based Full-Adder for Future VLSI Design", IEEE Transactions on Device and Materials Reliability 2016.

[7] Sambhu Nath Pradhan and Vivek Rai et al., "Design of High Speed and Low Power Full Adder in Subthreshold Region", IEEE 2016.

[8] Sudhakar Alluri and M.Dasharatha et al., "Design of Low Power High Speed Full Adder Cell with XOR/XNOR Logic Gates", International Conference on Communication and Signal Processing IEEE 2016.

[9] Krishnendu Dhar, "Design of a Low Power, High Speed, Energy Efficient Full Adder Using Modified GDI and MVT Scheme in 45nm Technology", International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT) IEEE 2014.

[10] Mayur Agarwal and Neha Agrawal, "A New Design of Low Power High Speed Hybrid CMOS Full Adder", International Conference on Signal Processing and Integrated Networks (SPIN) 2014.