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Modelling and Simulation of Low Power ALU Using Pass Transistor Transmission Line Logic

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Abstract- Full Adder, which is the core of any arithmetic and logic unit that is the main component used in all the processors. This correspondence presents a design technique using pass transistor logic (PTL) and transmission gates for the architecture of full adder with minimum number of transistor and reduced delay. It is then used to implement an ALU for carrying out arithmetic and logical tasks. The analysis of the developed ALU is done at 27°C and 100°C range in CMOS 90 nm, and 50 nm technologies using Micro wind tool. We also use Questa-sim to simulate the ALU. A comparison table will be shown having temperature based comparison at 90nm and 50nm technologies showing delay in time and dissipated Power within the ALU at both temperatures. We will also provide the layout of the ALU at both technologies.

Key words: Full Adder, PTL, ALU, Power, Delay.

I. INTRODUCTION

The respective deprecation of detention amount and power expenditure is turned into one in all the crucial drawback relating to implementation of the highest level completion of process units. Arithmetic and Logical Unit is a fundamental a part of each mainframe style. It attains arithmetical, Logical and Unary operations on integers unbroken in accumulator unit, register array, operand register and values fed from outer memory. In recent decades, numbers of designs are given for effective power handling capability and good performance. The implementation of an adder in parallel manner in ALU has become a very important role, as the propagation of respective (CP) is chargeable for the delay additionally. With the help of sacred writing arithmetic variety of operations will be performed in straightforward steps. The multiplier is the most delay inflicting unit, therefore the output of number affects the whole ALU unit. Further, it normally covers the most of space. Therefore, as a summary it will be aforesaid that improvement of the world and delay of the number uniting ALU may be a very important style issue.

On other hand, ALU is an essential a part of processor. It plays vital role in activity pure mathematics and logical operations on knowledge. All rest of the weather of system like control unit, register, memory, I/O are in the main accountable to bring knowledge into the ALU for method and then to require results back out. ALU is a combinational kind of circuit, which is in a position to perform entire register transfer operation from the supply register through ALU and into the destination register throughout one clock pulse amount. It is a basic building block of any microprocessor in conjunction with DSP processor that accomplish several arithmetic operate grounded upon the management input choice. ALU is the heart of any microprocessor system. ALU bring about basic arithmetic operate like addition, subtraction and logical functions including logical AND, logical OR, logical XOR etc. These different functions of ALU are collocates with the facilitate of set of basic units. Now a days, increasing demands of gadgets like laptop, tablets, PCs forcing technologies to develop high speed processor. [1] The speed of any processor is mainly relying upon procedure time must end the task in ALU. Adder and multiplier is main basic block within ALU on that speed is depended. The system can be created cheerful, a lot of economical and more versatile by reducing the range of core parts like adder and number within the electronic equipment. The ALU takes as input the data to be operated i.e. operands and a code from the control unit indicating that operation to be performed. The output is the results of the computation which we tend to are realizing. [2] VHDL is a very powerful language for the programming furthermore as for style purpose and at an equivalent time it's straightforward to infuse in conjunction with filled with Mysteries. Its benefit is that VHDL permits the description of a coincident system. VHDL project is multipurpose and moveable.

The VHDL software interface used in this style reduces the quality and additionally provides a graphic presentation of the system. [3] The key advantage of VHDL when used for systems style is that it permits the behavior of the needed system to be delineated and verified before synthesis tools interprets the look into real hardware (gates and wires). This software not solely compiles the given VHDL code however additionally generates wave results.

II. RELATED WORK

In paper [4] they designed, fabricated, and tested a 4-bit bit-slice ALU for 32-bit microprocessors using RSFQ circuits. The proposed ALU consists of 3481 Josephson junctions with an area of 3.09×1.66 mm^2. Simulation results showed that the ALU has DC bias margins of ±20%, a latency of 524 ps, and a throughput of 6.25×10^9 32-bit operations per second at the target operating frequency of 50 GHz. The width of the measured DC bias margins was around 10% at 50 GHz. The proposed ALU can be used for any 4n-bit processing. We successfully demonstrated high-frequency operation of the bit-slice ALU, comparable to that of a bit-serial ALU, via precise control of interconnect delays and clock distribution. They believe that their results demonstrate the potential of bit-slice processing for 32-bit RSFQ microprocessors. The optimal width of a slice depends not only on ALU performance but also on microprocessor system design (e.g. instruction execution control and memory bandwidth). They plan to investigate the slice width in their future work.

In paper [5], 8-bit ALU design using 11-T FA and GDI based multiplexer at 32nm technology. At 32nm technology high-k dielectric and metal gate is to be introduced. There are three main sources responsible for occurring leakage current are the gate direct tunneling current, the subthreshold leakage current and reverse biased junction leakage. High-k dielectric is permitted to increase the gate capacitance and reduced the leakage power due to gate direct tunneling current. Metal gate make better strain capacity. Subthreshold leakage current is to be used at subthreshold mode and consumes low power. Finally, 8-bit ALU performs better as compare to existing design and consumes low power.

In paper [6] it is described that an ALU with LUT multiplier for mobile GPU is proposed. The ALU is based on Approximated Precision Shader (APS). The LUT multiplier was compared with different multipliers regarding delay with various bits width. The proposed multiplier technique improves the speed multiplier by reducing the number of partial products. The ALU design has been simulated using Xilinx ISE and realized on Xilinx virtex-5XC5VLX30 FPGA. The proposed work gives an overall good performance compared with the conventional one.

In paper [7] the 8-bit ALU is designed using conventional CMOS and low power nano device SET. It is simulated in SPICE software and it is proved that the ALU using SET consumes much less power when compared to the conventional CMOS. This 8-bit ALU can be used in many digital processors to make it power efficient compared to the conventional processors.

In paper [8] a new design for an 8 bit ALU was proposed using reversible logic and implemented at the transistor level. The control circuitry was built solely using COG gates. The inputs of the HNG gate were modified to act as a full adder. These two units were combined to form the 1-bit ALU, which was further cascaded to form the 8-bit ALU. The gate count, number of constant inputs and number of garbage outputs are 6, 5 and 9 respectively. This was found to be lesser than that of the existing designs. The propagation delay was lesser than that of the existing design by 33.41%.

In paper [9] there is 82.48%, 73.54%, 67.54%, 61.95% and 62.82% IO power reduction for 0.9GHz, 2.4GHz, 3.6GHz, 4.9GHz and 5.9GHz frequencies respectively when they migrate from GTLP_DCI IO standard to GTL IO standard. There is total power reduction of 65.39% for 0.9GHz frequency when we migrate from GTLP_DCI to GTL IO standard. There is 55.98%, 50%, 42.99% and 37.73% reduction in total power for the frequencies 2.4GHz, 3.6GHz, 4.9GHz and 5.9GHz respectively when we migrate from GTLP_DCI IO standard to GTLP IO standard. Virtex-5 FPGA is used for the implementation of this Arithmetic Logic Unit (ALU) design. This Arithmetic Logic Unit (ALU) can be redesigned on Virtex-6, Virtex-7 and Airtex-7 FPGA. This technique can also be implemented to design low power single core processors and low power multicore processors.

In paper [10] it is described as a 16-bit arithmetic logic unit with 8 functions is designed and the design is validated using the schematic editor DSCH. The physical layout for the circuit is simulated using a software tool by Microwind, France. The 16-bit ALU design uses 4 bit carry skip adder modules as it gives the least power dissipation and comparable critical path delay for carry to be propagated compared to other 4 bit adder topologies considered. Different logic

families are preferred for each module so as to optimize the overall performance of the 16 bit ALU. The 16 bit ALU has been designed using a carry skip adder and optimized using mixed logic families in the design. In this paper, VLSI design of an optimum 16- bit ALU design is presented which utilizes the advantages of three different logic families such as CMOS, Pseudo NMOS and Pass Transistors. The Full Adder used in the ALU is designed using multiplexer based logic with 12 transistors. The design is optimized for an output load capacitance of 8pF. The Power-Delay product for the proposed design is 1.9477% lower than the CMOS design of the same ALU. The implementation of the different logic families in the same circuit has helped in optimizing the overall circuit performance in terms of delay and power consumption.

III. PROPOSED METHODOLOGY

The general proposed methodology has the following essential blocks module.

A. DSCH (Implement ALU using adder cell (PTL) and generate Verilog code for layout on micro-wind).
B. Micro-Wind (Layout of designing and gain, delay analysis).
C. Simulate the Verilog code on Questa-sim.

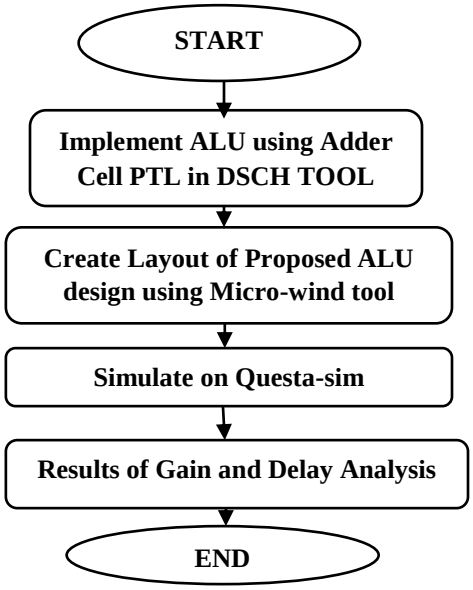

Figure 1 Overall Activity Perform of our Proposed Methodology

The above figure showing that the overall activity of our proposed methodology and also showing the all processes that are involved in this proposed methodology.

In this paper, an effort has been made to design and develop the ALU circuit by employing single rail lean PTL i.e. pass transistor logic method. The advantages of PTL come from the fact that it is best suitable to implement power reduction techniques.

IV. SIMULATION RESULTS

In this paper we have proposed an ALU design based on energy efficient low power area pass transistor logic employing 3 simulation software's. We employed DSCH for designing, Micro-wind for layout and power analysis and then Questa-sim for the behavior simulation and to obtain the waveform of results. The DSCH program is a logic simulator and editor package. Micro-wind is an innovative CMOS designing tool for academic areas. The Questa Advanced Simulator comprises enhance performance and capacity simulation with unified sophisticated debug and functional/operational coverage abilities for the almost complete native support of Verilog, System Verilog, System-C, VHDL, UPF, SVA, and UVM.

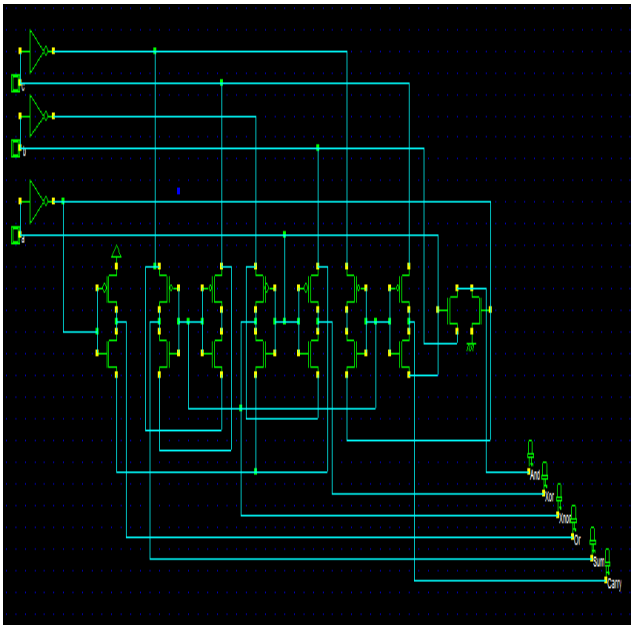

Figure 2 Implemented Design of Proposed 1-Bit ALU

Figure 2 showing the implemented design of 1-bit ALU in DSCH tool employing full adder using C-MOS inverter circuit.

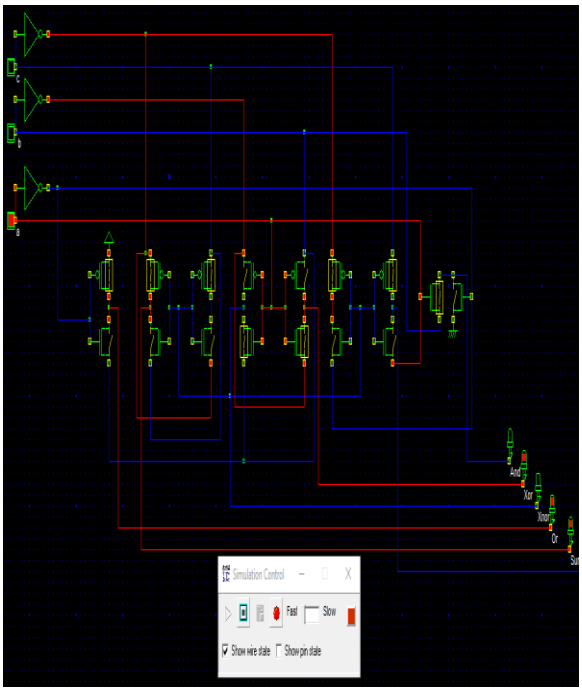

Figure 3 DSCH 1-Bit ALU Design Output Result when one input (a) is high (1)

Figure 3 illustrates the result of presented design of 1-bit arithmetic and logic unit when one of the 3 inputs is high i.e. 1, while remaining 2 are low.

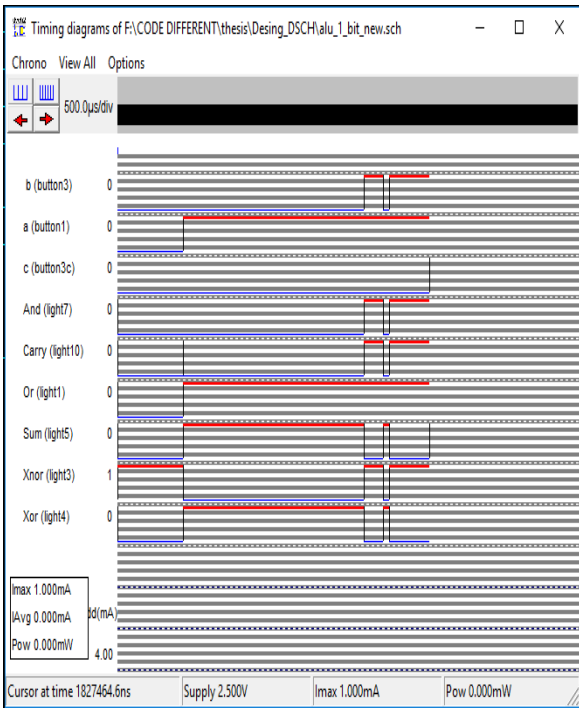

Figure 4 Timing Diagram of DSCH 1-Bit ALU Design

Figure 4 illustrating the Timing Diagram of DSCH 1-Bit ALU Design.

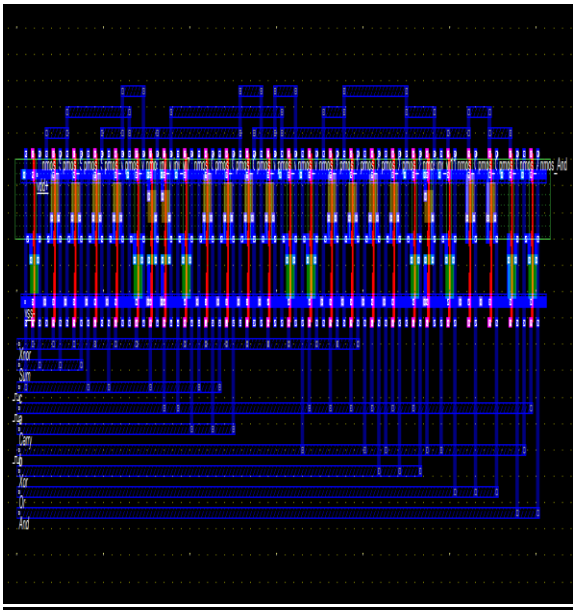

Figure 5 Layout of 1 Bit ALU on Micro-wind

Figure 5 illustrating the layout of 1 Bit ALU on Micro-wind.

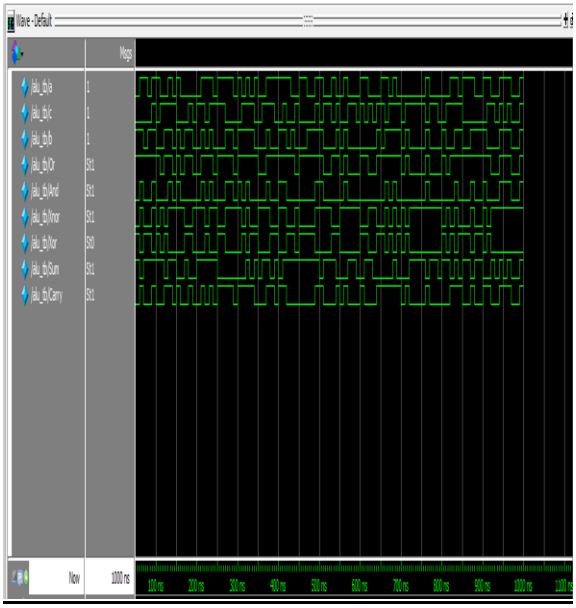

Figure 6 Shows the Waveform of 1-Bit ALU on Questa-sim

Figure 6 illustrating the Waveform outcome of 1-Bit ALU on Questa-sim software package.

Table I Comparison of Simulation Results of the 1-Bit ALU Design

ALU Design	8T FA & PTL	Power Gating Technique	Proposed Design
Propagation Count Delay (ns)	101.10	50.10	50.1
Average Power Consumption(μW)	261.10	160.10	4.34
Number of Transistor	12	13	16

The table I shows the comparison between few existing designs and the presented architecture of 1-Bit ALU Design on the basis of certain parameters taken into consideration such as propagation count delay, average power consumption etc. The table evidently indicates the advantages of the presented architecture.

V. CONCLUSION

This design using PTL consumes minimum of short circuit power. There is no static leakage in the PTL architecture, as there is no direct path from V_{DD} to GND. This particular architecture follows all the design protocols of the PTL precisely, it has no Glitching power consumption as the delays can be monitored by controlling W/L ratios. There is no high impedance state in the proposed circuit when compared to the earlier design. Because of all the above discussed qualities this circuit consumes less power and architecture is extremely simple. With this low power design and PTL implementation there is overall reduction in power dissipation in total by 98 % and 97% when compared to previous ALU design.

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