A Literature Review on High Speed Area Efficient Using Different Energy Efficient Approaches

[1]Priyanka Bharadwaj, [2]Ashish Raghuwanshi
[1]M-Tech Scholar, [2]Assistant Professor,
Department of Electronics & Communication Engineering, IES, Bhopal
damini2605@gmail.com, ashishraghuwanshi.06@gmail.com

ABSTRACT- In this paper, Authors have presented the literature on coming up with of high speed, less area 64-bit ALU using economical techniques. The optimization of the projected style can be done by using the various techniques. The parameters speed and area of the projected style can be improved by using Carry Look Ahead Techniques. It also reduces the circuit quality. The ALU is a fundamental building block of central process unit of a laptop that is employed within the simplest microprocessors for purpose of maintaining timers. Previously, much economical design has been introduced for the style of low quality operation, but we tend to have given the attention to the carry look ahead and reversible gate techniques. The proposed style of ALU can performs the mathematical, logical, and shifting operations like Addition, Subtraction, Multiplication, Increment, Decrement, Logical AND, Logical OR, Logical XOR etc. in the computer. In this paper, the efficient modules of ALU are style using Xilinx package and simulation results can be verified on same platform exploitation check benches.

KEYWORDS: ALU, XILINXS, VHDL, VERILOG, COPLEXITY, SIZE

I INTRODUCTION

The respective deprecation of detention amount and power expenditure is turned into one in all the crucial drawback relating to implementation of the highest level completion of process units. Arithmetic and Logical Unit is a fundamental a part of each mainframe style. It attains arithmetical, Logical and Unary operations on integers unbroken in accumulator unit, register array, operand register and values fed from outer memory. In recent decades, numbers of designs are given for effective power handling capability and good performance. The implementation of an adder in parallel manner in ALU has become a very important role, as the propagation of respective (CP) is chargeable for the delay additionally. With the help of sacred writing arithmetic variety of operations will be performed in straightforward steps. The multiplier is the most delay inflicting unit, therefore the output of number affects the whole ALU unit. Further, it normally covers the most of space. Therefore, as a summary it will be aforesaid that improvement of the world and delay of the number uniting ALU may be a very important style issue.

On other hand, ALU is an essential a part of processor. It plays vital role in activity pure mathematics and logical operations on knowledge. All rest of the weather of system like control unit, register, memory, I/O are in the main accountable to bring knowledge into the ALU for method and then to require results back out. ALU is a combinational kind of circuit, which is in a position to perform entire register transfer operation from the supply register through ALU and into the destination register throughout one clock pulse amount. It is a basic building block of any microprocessor in conjunction with DSP processor that accomplish several arithmetic operate grounded upon the management input choice. ALU is the heart of any microprocessor system. ALU bring about basic arithmetic operate like addition, subtraction and logical functions including logical AND, logical OR, logical XOR etc. These different functions of ALU are collocates with the facilitate of set of basic units. Now a days, increasing demands of gadgets like laptop, tablets, PCs forcing technologies to develop high speed processor.[1] The speed of any processor is mainly relying upon procedure time must end the task in ALU. Adder and multiplier is main basic block within ALU on that speed is depended. The system can be created cheerful, a lot of economical and more versatile by reducing the range of core parts like adder and number within the electronic equipment. The ALU takes as input the data to be operated i.e. operands and a code from the control unit indicating that operation to be performed. The output is the results of the computation which we tend to are realizing.[2] VHDL is a very powerful language for the programming furthermore as for style purpose and at an equivalent time it's straightforward to infuse in conjunction with filled with Mysteries. Its benefit is that VHDL permits the description of a coincident system. VHDL project is multipurpose and moveable. The VHDL software interface used in this style reduces the quality and additionally provides a graphic presentation of the system. [3] The key

advantage of VHDL when used for systems style is that it permits the behavior of the needed system to be delineated and verified before synthesis tools interprets the look into real hardware (gates and wires). This software not solely compiles the given VHDL code however additionally generates wave results.

II EXISTING WORK ON EFFICIENT ALU MODULE

In In 2016 IEEE H. V. Ravish Aradhya et al. [4] presented an article. In this article proposed, the advancement of transistor method technology reduces the chip space at the value of power consumption. Adiabatic logic is one of the promising low power techniques, which offers low power dissipation at the price of delay. The proposed work optimizes delay using MOS-GNRFET as the device rather than Si-MOSFET and proposes ECRL logic primarily based 8-bit ALU design activity four arithmetic and four logical operations. The Kogge-stone parallel adder structure is used within the ALU to cut back delay as a result of the pipelined architecture of ECRL and lower range of stages in kogge-stone adder. ALUs in CMOS, ECRL and GNRFET-ECRL have been designed for 10nm process technology and are simulated using H-spice. The CMOS, ECRL and GNRFET-ECRL ALUs are having power dissipation values of 38.75mW, 14.131 mW and 158.799 nW severally.

In 2016 IEEE Deeptha A. et al. [5] proposed an article. In this article proposed, Conventional Complementary metal compound semiconductor circuits (CMOS) dissipate energy in the type of bits of knowledge. This dissipation of energy is in the type of power dissipation and plays a really important role as way as low power style is taken into account. Today, most digital circuits are being designed using Reversible Logic. Design primarily based on Reversible Logic helps in reducing heat dissipation, allowing nearly energy free computation, allowing higher circuit densities and enabling higher testing of faults. In this paper, a novel design for a Reversible 8-bit ALU is planned. The 8-bit ALU is designed by cascading 1-bit ALUs. The two major units of a 1-bit ALU are the control unit and therefore the adder unit. For the control unit, the Control Output Gate (COG) has been used and for the adder unit the Haghparast and Navi Gate (HNG) has been used. The most significant facet of this paper is that as compared to alternative papers, this ALU design has reduced gate count, and transistor count. The propagation delay was found to be significantly lesser at a worth of five.52ns when compared with the worth of 8.29ns for an existing style. Simulation and verification of

the proposed style was performed using Cadence 180nm technology computer code tool.

In 2016 IEEE Anitesh Sharma et al. [6] presented an article. In this article presented, Arithmetic logic unit (ALU) is an vital a part of silicon chip. In digital processor logical and arithmetic operation executes using ALU. In this paper we describes 8-bit ALU using low power 11-transistor full adder (FA) gate diffusion input (GDI) primarily based electronic device. By using solfa syllable and electronic device, we have reduced power and delay of 8-bit ALU as compare to existing style. All design were simulated using Tanner EDA tool v15.0 in 32nm BSIM4 technology. Performance analyses were done with relevancy power, delay and power delay product.

In 2015 IEEE Madhavika Agrawal et al. [7] proposed AN article. In this article proposed, Wi-Fi Enable ALU on 90nm primarily based Virtex-4 FPGA is analyzed using thermal scaling and frequency scaling. It is Wi-Fi enable as a result of we have a tendency to are operative our ALU with frequencies of various IEEE 802.11 Wi-Fi Channel. Frequency scaling and temperature scaling results in power consumption variation and eventually saving of energy. Clock power, logic power; signal powers, IOS power, leakage power all are dependent on frequency and temperature. The ALU is analyzed to work with efficiency at Wi-Fi channel ah, having frequency around 0.9GHz. We are additionally achieving reduction in vary of 30-60% for outflow power using frequency scaling and thermal scaling. For further reduction of power dissipation at high frequency vary, we are additionally using totally different Clock Gating techniques.

In 2015 Neha Agrawal et al. [8] proposed a paper. In this paper proposed, we have tried to create energy economical ALU on 90nm primarily based Virtex-4 FPGA using totally different a hundred and ten standards, as with the scaling of technology power dissipation has become a serious concern for prime performance ALU design. As 50% of the total power of ALU is dissipated solely in clock and 1/0 pads, hence in order to create it energy economical clock gating technique is introduced and therefore the analysis of power dissipation has taken on totally different 1/0 standards. It is Wi-Fi enable as a result of we have a tendency to be operative our ALU on frequencies of various IEEE. We are analyzing the worth of power dissipation using different or totally different or completely different a hundred and ten standards and on different Wi-Fi channel frequencies. We are achieving reduction in total power dissipation to ninety five.13% with LVCMOS15 and 95.18%

with LVDCI_15 and once introducing Clock Gating we have a tendency to be achieving reduction in total power dissipation to 95.35% with LVCMOS_15 and 94.99% with LVDCI_15.

In 2016 KartiK Kalia et al. [9] proposed an article. In this article proposed, consists of design primarily based on property energy economical ALU32Bit and for that reason we've got used four totally different members of GTL IO standards on 65nm technology. In this paper, we have thought-about 2 main parameters for analysis that are frequencies in ghz and airflow (LFM 250). We have thought-about

Medium as a default profile for warmth sink and atmosphere is constant. Xilinx is used for the simulation of logic with Verilog as hardware description language. We have done our analysis for various frequency values for WLANs supported IEEE 802.11 standards. When we have a tendency to scale down from 60GHz to 0.9 GHz we have a tendency to discovered most IO power reduction and outflow power reduction in GTL, constant clock power and logic power reduction in all the considered IO standards and most Signal power reduction in GTLP_DCI and GTL_DCI.

Table no. 1 Brief literature survey contribution of research work methodology

S. No.	Ref. No.	Author	Publication	Year	Methodology	Contribution
1	04	H. V. Ravish Aradhya et al.	IEEE	2016	MOS-GNRFET	The advancement of transistor method technology reduces the chip space at the price of power consumption. Adiabatic logic is one of the promising low power techniques, which offers low power dissipation at the value of delay. The proposed work optimizes delay using MOS-GNRFET as the device rather than Si-MOSFET and proposes ECRL logic primarily based 8-bit ALU design activity four arithmetic and four logical operations.
2	05	Deeptha A. et al.	IEEE	2016	cascading 1-bit ALUs, COG	The most significant facet of this paper is that as compared to different papers, this ALU design has reduced gate count, and transistor count. The propagation delay was found to be significantly lesser at a worth of 5.52ns when compared with the worth of eight.29ns for an existing style. Simulation and verification of the proposed style was performed using Cadence 180nm technology software system tool.
3	06	Anitesh Sharma et al.	IEEE	2016	low power 11-transistor full adder (FA) and Gate diffusion input (GDI) based multiplexer	We have reduced power and delay of 8-bit ALU as compare to existing style. All design were simulated using Tanner EDA tool v15.0 in 32nm BSIM4 technology. Performance analyses were done with relevance power, delay and power delay product.
4	07	Madhavika Agrawal et al.	IEEE	2015	Wi-Fi Enable ALU	We are additionally achieving reduction in vary of 30-60% for outflow power using frequency scaling and thermal scaling. For further reduction of power dissipation at high frequency vary, we are additionally using totally different Clock Gating techniques.
5	08	Neha	IEEE	2015	LVCMOS_15,	We are achieving reduction in total

		Agrawal et al.			LVDCI_15 ,	power dissipation to 95.13% with LVCMOS15 and 95.18% with LVDCI_15 and once introducing Clock Gating we tend to are achieving reduction in total power dissipation to 95.35% with LVCMOS_15 and 94.99% with LVDCI_15.
6	09	KartiK Kalia et al.	IEEE	2016	AIRFLOW (LFM 250)	We have done our analysis for various frequency values for WLANs supported IEEE 802.11 standards. When we tend to scale down from 60GHz to 0.9 rate we tend to ascertained most IO power reduction and outflow power reduction in GTL, constant clock power and logic power reduction in all the considered IO standards and most Signal power reduction in GTLP_DCI and GTL_DCI.

III GENERAL PROPOSED METHODOLGY

Full Adder is a heart of any arithmetic and logic unit that is a fundamental element used in all the processor. The work proposes a design methodology using pass transistor and transmission gates for the designing of full adder with minimum number of transistor i.e. reduced size and reduced delay. This is then used to implement an ALU performing arithmetic and logical tasks. The Analysis of the designed ALU is done at 27 C and 100 C temperature range in CMOS 90 nm, and 50 nm technologies using Micro wind tool.

The result shows the comparison between different CMOS technologies and temperature effect on the design in terms of delay and power dissipation.

A comparison is also done in terms of delay of the designed adder with previously ALU, which shows the advantage of the ALU design.

Tools used:-

1. DSCH
2. Micro wind
3. Xilinx ISE for RTL
4. Questa-sim for Simulation.

Firstly the adder cell will be implemented.

Using the adder cell we will implement the ALU in DSCH tool.

Then the Verilog code of the design is made and the layout will be made at CMOS 90 nm and 50 nm technology.

The design will be simulated for both 27 and 100 degree temperature.

RTL if needed will be designed in Xilinx ISE.

We can also use Questa-sim to simulate the ALU.

A comparison table will be made showing.

Temperature based comparison at 90 and 50 nm technology showing Delay and Power Dissipated in the ALU at both temperatures. We will also provide you the layout of the ALU at both technologies.

IV CONCLUSION

The efficient module of the ALU has been mentioned. After totally learning these literatures we have a tendency to have concluded that the techniques that non-heritable are far more effective to enhance the parameters of designed module of 64-bit ALU. These help in optimizing the system by using economical techniques. The ALU design using carry look ahead and reversible logic gate approach will increase the speed to an excellent extent but it will increase the hardware complexness. The proposed methodology provides systematic thanks to derive high speed system at a really less space. We have projected the model of 32 bit and 64 bit ALU with economical style approach victimization less space, high speed methodology. Also, Author efforts will be directed towards implementation of sixty four bit ALU style with totally different circuit topology and optimization.

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