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Designing and Simulation of High Speed Area Efficient Full Adder Using Pass Transistor Logic

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Abstract- Full Adder is the heart of any central processing unit that is a core component employed in all the processors. This thesis presents a design methodology using pass transistor logic and transmission gates for the architecture of full adder with minimum number of transistor i.e. reduced size and reduced delay. This is then used to implement a full adder design for carrying out arithmetic and logical tasks. The analysis of the developed full adder design is done at 27°C and 100°C range in CMOS 50 nm technologies using Micro wind tool. The result shows the comparison between different CMOS technologies and temperature effect on the design in regards of delay in time and power dissipation. A comparison is also carried out by some of the parameters taking into consideration like delay of the proposed adder with existing full adder design, which shows the advantage of the full adder design. We are using different simulation tools like Micro-wind-DSCH and Questa-sim for waveform simulation. Firstly the adder cell will be implemented using DSCH tool. Then the Verilog code of the design is made and the layout will be made at CMOS 50 nm technology. The design will be simulated for both 27°C and 100°C temperature. We also use Questa-sim to simulate the full adder design. A comparison table will be shown having power, delay and transistor count based comparison at 50nm technologies showing delay in time and dissipated Power within the full adder design at both temperatures. We will also provide you the layout of the full adder design at both technologies.

KEYWORDS: FA, CMOS, Micro-Wind, DSCH, Power, Delay.

I INTRODUCTION

Power consumption may be a key limitation in several electronic systems, starting from mobile telecommunication to transportable and desktop computing systems. Power is additionally a show stopper for several rising applications like close intelligence and detector networks. Consequently, new design methodologies and techniques are needed to regulate and control power dissipation. From refined handheld devices to bio- electronic circuits and Nano-satellites, all need low power style. Due to scaling, circuits have become a lot of capable, use a lot of transistors to implement difficult functions and supply new applications to customers. However this implies a lot of power consumption. In some cases, low power style is needed to avoid overheating. There are alternative applications like bio-electronics wherever the circuit would be constituted within the body and has got to work either with small battery or victimization power harvest home techniques. Kind of like that, RFID and growing detector networking circuits even have to consume terribly low power owing to out there power limitation.

In some cases we have a tendency to could contemplate low-power style a second priority, however in those applications lower-power style is important. Thus either supply power limitation or, over heating concern and battery life thought, low power style is that the answer.

To own low power digital processing, a low-power full adder is desired. In terms of power dissipation techniques and also comparison there are few papers and references available. At the design level, some solutions like adiabatic circuits are introduced to reduce power consumption. However, a number of these solutions, like adiabatic, may not be practical as a result of the quantity of transistors they need. A number of these techniques like pipeline structures or asynchronous temporal order turning into additional engaging and obtaining additional attention than other solutions. This is often beside the first and main resolution to cut back the availability voltage. The aim of this analysis is to explore completely different solutions together with circuit techniques and to achieve a sensible low-power design.

A combinational circuit consists of logic gates whose outputs at any time are determined directly from the present combination of inputs without regard to previous inputs. The combinational logic circuit performs a specific information processing operation fully specified logically by a set of Boolean functions. The combinational circuit consists of input variables, logic gates and output variables. The logic gates accept signals from the inputs and generate signals to the outputs. This process transforms binary information from the given input data to the required output data. Therefore, both input and output data are represented

by binary signals, i.e., they exist in two possible values, one representing logic-0 and the other logic-1. Any combinational circuit can be designed by the following design procedure:

1. Identify the number of input variables and required output variables.
2. Assign letter symbols to input and output variables.
3. Derive the truth table that defines the required relationship between input and output variables.
4. Obtain the simplified Boolean functions for each output variable by using K-map.
5. Draw the logic diagram for above simplified expression by using logic gates.

Digital computers and calculators consist of arithmetic and logical circuits that add, subtract, multiply and divide binary numbers. The basic combinational circuits are arithmetic circuits. In this thesis, three different single bit arithmetic structures are presented. They are adders, subtractors and multipliers. These structures are popular designs in the transistor technology.

II RELATED WORK

This paper [1] introduce Quantum Dot Cellular automata, one of the emerging nanotechnology is the possible alternative to these problems. This paper presents the comparative analysis of various QCA methodologies used for the implementation of full adder circuit. Also the designs and performance analysis of QCA full adder using Majority gate, minority gate, multilayer wire crossing, 5 input Majority voter gate is discussed. The designs follow the conventional design approaches, but due to the technology differences, they are modified for the best performance in QCA. The layout and simulation results are presented using QCA Designer Tool. QCA Designer is a QCA layout and simulation tool developed at the University of Calgary. Simulations indicate very attractive performance regarding complexity, area, and delay in Minority gate based full adder and 5 input MV gate based full adder.

The research [2] describe the limitations of complementary metal–oxide– semiconductor (CMOS) technology on the nanoscale will prevent continuation of the current scaling trends in very large-scale integration (VLSI). Quantum-dot cellular automata (QCA) are one of the emerging nanotechnologies, conceived as a viable alternative to CMOS circuits, offering exceptionally high integration density, impressive switching frequency, and remarkably low power characteristics. However, fabrication issues and susceptibility to high error rates have raised many questions regarding this technology, leading to the search for efficient and scalable methods for design of QCA circuits. In this regard, this work targets a generic, reliable and programmable (RP) architecture for QCA with hybrid cell orientation. An efficient, easily manufactural, and scalable clocking scheme is proposed towards the design of fault-tolerant QCA architectures. The functionality and defect tolerance of a five-input majority voter with RP structure (RMV) are investigated under cell deposition defects. Simulation results demonstrate that the proposed RP structure is more reliable than the conventional design. Besides reliability, the most striking characteristic of this logic is that it is completely programmable to perform various logic functions, reducing the requirement for disparate logic for large circuits. Comprehensive analysis of its programmable feature is applied to achieve a full adder, which extends its reliability to circuit level. The design of the QCA layout, as well as functional verification of the proposed design, is performed using QCA Designer.

The research [3] introduce that the full adder cells play a vital role in numerous VLSI circuits. Therefore, design of an energy-efficient full adder which operates reliably in submicron technologies has become a great concern in recent years. Some previously designed cells suffer from non-full swing outputs, high-power consumption and low speed issues. In this paper, two high-speed, low-power and full swing full adder circuits are designed in 90-nm CMOS technology. According to simulation results, the proposed circuits have rail to rail output signals. Also, an improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay, power consumption and power-delay product (PDP), respectively.

In this paper [4], hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve Low power and high speed. Hybrid logic style used is the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The Circuit was implemented using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA) and Transmission Function adder (TFA). Average Power consumption of the proposed design is found to be 1.114 μW at 90nm for 1.2V supply and 5.641 μW at 180nm for 1.8Vsupply. Delay in the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies respectively. Thus consuming extremely low power and requires less time than existing designs for the same testing environment. Power Delay Product (PDP) is calculated as product of Power and delay values signifies energy requirement of the design. Proposed design requires 71% less energy than

TFA and 81% less energy than TGA and 92% less energy than conventional CMOS adder.

The research article [5] proposed that the designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is array multiplier. Array multiplier half adder have been used to sum the carry products in reduced time. Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier, which is the major power consuming element in the digital circuits. Basically the process of multiplication is realized in hardware in terms of shift and add operation. The optimization of adder has led to the improvement in performance of multiplier. In this paper, a modified full adder using multiplexer is proposed to achieve low power consumption of multiplier. To analyze the efficiency of proposed design, the conventional array multiplier structure is used. The designs are developed using Verilog HDL and the functionalities are verified through simulation using Xilinx. The ASIC synthesis results of the proposed multiplier shows an average reduction of 35.45% in power consumption, 40.75% in area, and 15.65% in delay compared to the existing approaches.

In this paper [6] introduce the modern nanotechnology and quantum computation, reversible logic plays a pivotal role as it has minimal impact on physical entropy. Reversible logic gates have same number of input and output hence power loss due to bit erase operation can be avoided. There are many reversible logic structures which can perform different Arithmetic and logic operations as traditional or classical logic structures can do. In this paper, two reversible logic structures are proposed which can perform operation of addition. These logic structures namely proposed design I and Proposed design II, generate carry output signal and carry propagate signal on the basis of two reversible logic gates known as Fredkin gate and Feynman gate. Performance of proposed designs is evaluated in terms of quantum cost, constant input, garbage output and delay. It is found that proposed design II is a better choice over proposed design I and some other existing Designs.

The Paper [7] discussed the comparative analysis of different Fin-FET based full adder cells designed with various logic styles. The logic styles used for implementation of Fin-FET based 1-bit full adder are Complementary MOS (CMOS), Transmission Gate (TG) and Complementary Pass-Transistor Logic (CPL). The simulations have being done at 10nm, 20nm and 32nm technology node for all full adder cell designs. PTM models for multi-gate transistors (PTM-MG) low power are used for simulations. The performance parameters that were measured, analyzed and compared are average power, leakage power, delay, and energy. It is observed that less power is consumed in Transmission Gate (TG) based full adder than the Convention full adder and complementary pass-transistor logic (CPL) based full adder in 10nm technology node. Also, found reduction in delay, EDP, and PDP in TG based full adder compared to other cell designs.

The paper [8] very large-scale integrated circuit (VLSI) design, based on today's CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of non-volatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. They also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full non-volatility for future nonvolatile microprocessors.

The research [9] introduce the solution of the serious problem of threshold loss that causes non-full-swing at the out-put of 1-bit full adder, an arrangement in which all the transistors are forced to operate in sub-threshold regime is proposed in this paper. But this will in turn bring additional area and delay overhead. In this work, full swing at the output of 1-bit full adder is retained with reduced area and delay overhead. An additional capacitor working in the differential voltage mode will be replacing the transistor that is used to reduce the threshold loss problem at the output of 9T based full adder as discussed in this paper. Previous works related to this domain concerns about reduction of power of only 1-bit adder. The work targets power and area reduction of 1/4/8/16 bit adders. Proposed adder shows maximum total power saving of 46.87 % and 25.99 % with respect to 8T and 9T adder configurations respectively.

This paper [10] present, a three transistor XNOR gate. The proposed XNOR gate is designed

using CADENCE EDA tool and simulate using the SPECTRE VIRTUOSO at 180 nm technology. The proposed results are compared with the previous existing designs in term of power and delay. It is observed that the power consumption is reduced by 65.19% for three transistor XNOR gate and 48.11% for eight transistor full adder. It is also observed that the delay is reduced by 31.82% for three transistor XNOR gate and 28.76% for eight transistor full adder. This paper [11] proposes the design of a low power, high speed, and energy efficient full adder using modified Gate Diffusion Input (GDI) and Mixed Threshold Voltage (MVT) scheme in 45nm technology. The proposed design on comparison with the traditional full adder composed of CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), respectively, exhibited a considerable amount of reduction in terms of average power consumption (Pavg), peak power consumption (Ppeak), delay time, power delay product (PDP), energy delay product (EDP) as well as transistor count and hence surface area. Pavg is as low as 7.61x10-7 watt while Ppeak is as low as 6.21x10-5 watt, delay time is found to be 2.05nano second while PDP is computed to be as low as 1.56x10-15 Joule and EDP is evaluated to be as low as 3.20x10-24 Js for 0.9 volt power supply. The simulation of the proposed design has been performed in HSPICE and the layout has been designed in Micro-wind.

In this paper [12] they have designed the full Adder using hybrid-CMOS logic style by dividing it in three modules so that it can be optimized at various levels. First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. It also consumes minimum power and provides better delay performance. Second module is a sum circuit which is also a XOR circuit and uses carry input and the output of the first module as input to generate sum output. Third module is a carry circuit which uses the output of the first stage and other inputs to generate carry output. In the new full adder design we have proposed new full adder circuit which reduce the power consumption, delay between carry out to carry in and PDP by 12 to 100%. Simulations are carried out on HSPICE using TSMC 0.18 μm CMOS technology..

III PROBLEM STATEMENT

Performance factors such as power, delay, and layout area were evaluated with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS output drive full adder. Due to toughness beside CMOS scaling and transistor sizing with the overhead of high input capacitance and requirement of buffers, the adder using this static CMOS. Also this design proves the power dissipation cause due to the stray capacitances and large length interconnects. The circuits design using CMOS logic with large number of transistors and maximum length interconnect are gradually more existing provider to propagation delay, overall area and power consumption. The main goal of this work is to improve the different function parameters such as power dissipation, path propagation delay and number of transistor used in full adder design compared with the previously existing ones.

Floating point (F.P.) addition is a preferable operation for a wide range of applications. The main areas in which they work are area-efficient, dynamically configurable, multi precision architecture for F.P. addition. In our work the use of transmission gate decreases the number of transistors which overcomes the area tradeoffs. The main drawback of the parallel adder is that the delay rises linearly with the bit length. Hence planned design will have:

- How circuit components get integrate?
- How to design and implement Dynamic CMOS gates and a set of experiments and results considering the features of the implemented gates.
- Representation of wiring connectivity in adder circuit.
- Presentation of every gate level property like truth table.
- Representation of connectivity of gates.
- For floating point numbers we design a power and area efficient adder.
- To overcome slow speed of a parallel adder and propagation delay of the carry.
- The main drawback of the parallel adder is that the delay rose linearly with the bit length.

IV PROPOSED WORK

The general proposed methodology has the following essential blocks module.

A. DSCH (Implement full adder using (PTL) and generate Verilog code for layout on micro-wind).
B. Micro-Wind (Layout of designing and gain, delay analysis).
C. Simulate the Verilog code on Questa-sim.

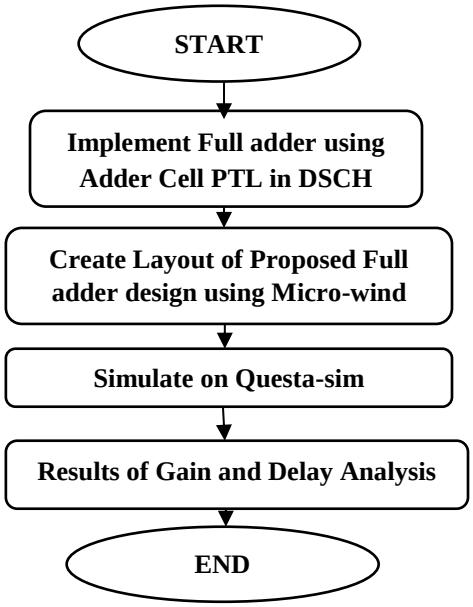

Figure 1 Overall Activity Perform of our Proposed Methodology

The above figure showing that the overall activity of our proposed methodology and also showing the all processes that are involved in this proposed methodology.

In this paper, an effort has been made to design and develop the full adder circuit by employing single rail lean PTL i.e. pass transistor logic method. The advantages of PTL come from the fact that it is best suitable to implement power reduction techniques.

V SIMULATION RESULTS

In this paper we have proposed full adder design based on energy efficient low power area pass transistor logic employing 3 simulation software's. We employed DSCH for designing, Micro-wind for layout and power analysis and then Questa-sim for the behavior simulation and to obtain the waveform of results. The DSCH program is a logic simulator and editor package. Micro-wind is an innovative CMOS designing tool for academic areas**.** The Questa Advanced Simulator comprises enhance performance and capacity simulation with unified sophisticated debug and functional/operational coverage abilities for the almost complete native support of Verilog, System Verilog, System-C, VHDL, UPF, SVA, and UVM.

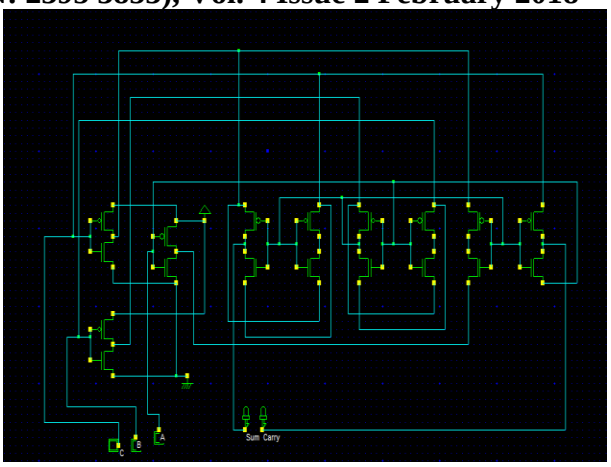

Figure 2 Implemented Design of Proposed Full Adder Module

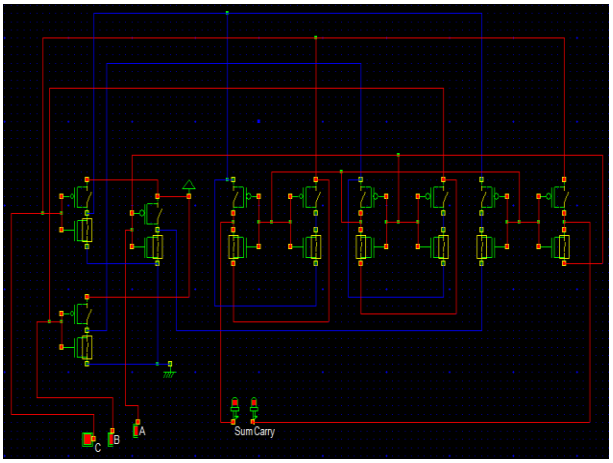

Figure 3 DSCH Full Adder Design output Results when all inputs are high (1)

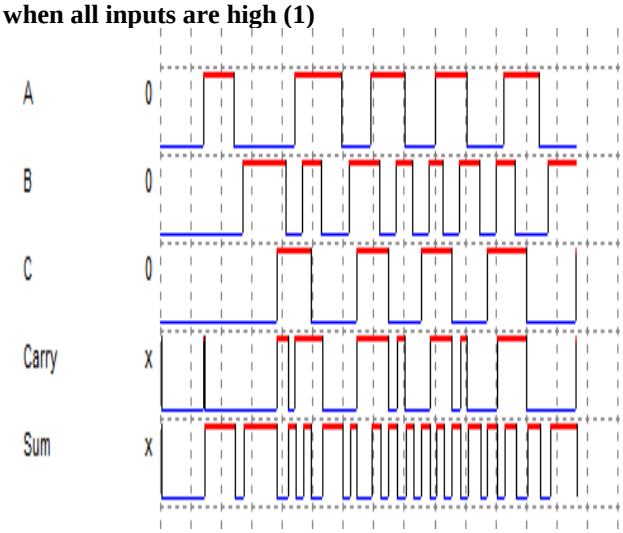

Figure 4 Overall Timing Diagram of DSCH Full Adder Design

Figure 2 show that proposed full adder design implemented in DSCH tool and figure 3 depicted the DSCH full adder design output results when two inputs are high (1) and figure 4 depicted that the timing

diagram of proposed full adder design in DSCH that the overall output results of full adder design in DSCH.

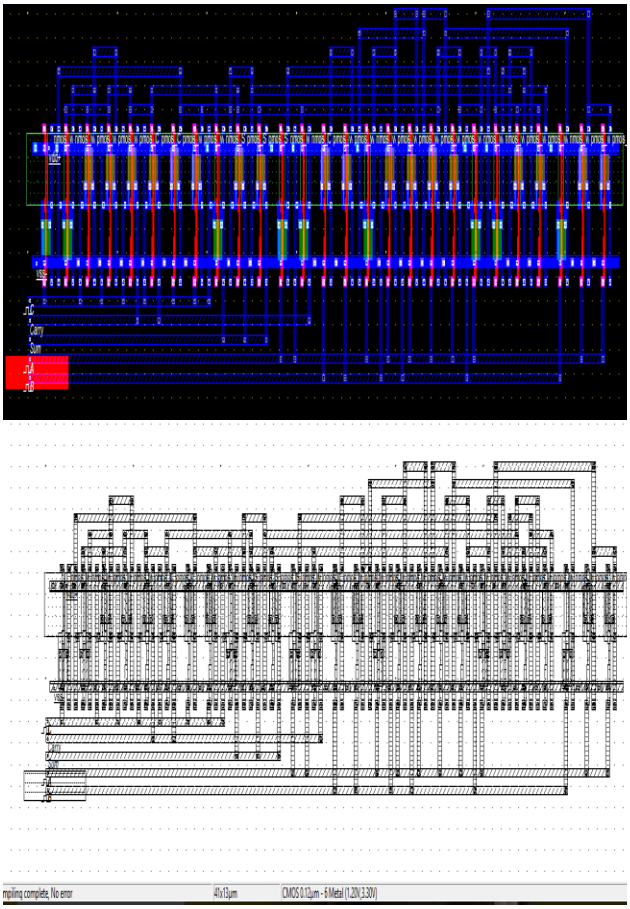

Figure 5 Layout of Proposed Full Adder Design in Micro-wind

In figure 5 we shows that the layout design of proposed full adder design which was generated in micro-wind layout tool.

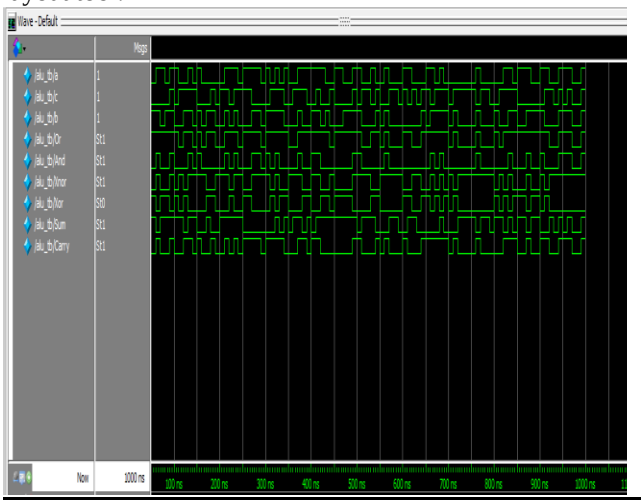

Figure 6 Shows the Simulated Timing Waveform of Proposed Full Adder Design

Comparative Analysis of Results

Table no. 1 Comparison of Simulation Results of Full Adder Designs

Full Adder Design	Conventional Design	Chaudhary Design	SERF Design	Proposed Design
Count Delay(ns)	0.366	0.513	0.39	0.33
Average Power Consumption(µW)	52.40	17.40	18.20	13.89
Number of Transist	28	8	10	8

The table 1 shows the comparison between few existing designs and the presented architecture of Full Adder on the basis of certain parameters taken into consideration such as count delay, average power consumption etc. The table evidently indicates the advantages of the presented design.

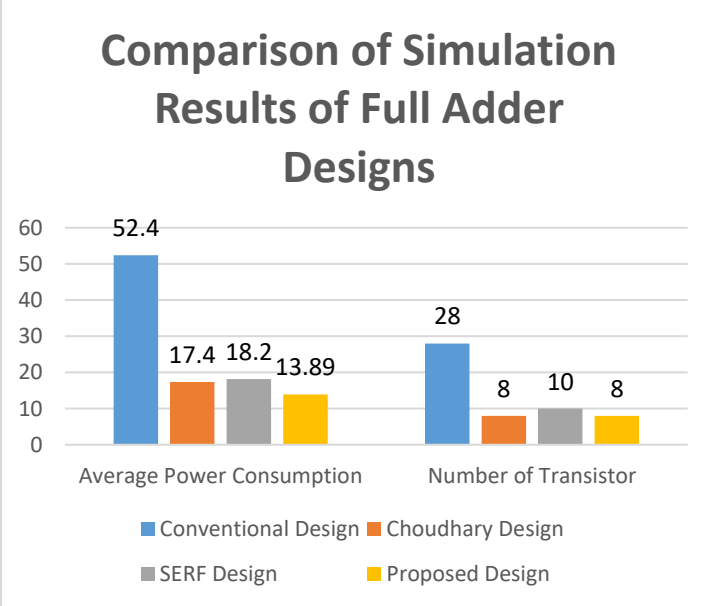

Figure 7 Chart shows the Comparison of Simulation Results of Full Adder Designs

VI CONCLUSION

In the proposed low power full adder cell, the total numbers of transistors are 8. And all the transistors used have minimum area transistor as far as size is concern that is there in the technology library. By the virtue of the transistor's small sizes there will be lower

IR drop that will dissipate across the given transistor. Best features and merits of the given 1 Bit full adder circuit when compared to other designs. The lower value of switching capacitance at the node in contrast to the traditional CMOS design, due to smaller size of the transistor. The fewer ground connections at the level restoring circuits and/or inverter buffers only i.e. less number of V_{DD} to GND connections throughout switching. So theoretically this design using PTL design must consume minimum quantity of short circuit power. There is no static outflow in the PTL architecture, as there is no direct path from V_{DD} to GND. The particular architecture follows all the design protocols of the PTL precisely, it is no Glitching power consumption as the delays can be monitored by controlling W/L ratios. There is no high impedance state in the proposed circuit when compared to the earlier design. Because of all the above discussed qualities this circuit consumes less power and architecture is extremely simple. With this low power design and PTL implementation there is overall reduction in power dissipation in total by 98 % and 97% when compared to previous full adder design. Pass transistor logic is advantageous for its simplicity. Although due to decreased transistor count both delay and power consumption will be lesser than other techniques, but the output is taken from diffusion output thus will lead to noise corruption and glitches at the output node. This issue may lead to functional failure down the path. However one can use inverter buffers to overcome the issue of signal degradation.

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