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Implementation of Energy Efficient SOC for AMBA-APB Protocol Using Memory Element

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Abstract- The fundamental assignment for a layout engineer is not handiest to layout a success SOC with a well-structured and synthesizable RTL code but also to layout it with low consumable in electrical power or energy and also optimized in electrical power or energy consumption. In this paper discusses the implementation of AMBA-APB bridges with high energy saving concept i.e. clock skew minimization technique. Clock skew should be major factor for any digital electronic device that also responsible for power consumption if system responded slowly define by delay of the system. There were several method or technique present by the researchers but have some limitation. In this paper introduces the new concept for clock slew minimization using memory element i.e. flip flop. This paper discusses the master-slave concept for memory element J-K flip flop. For implementation of this present approach using Verilog HDL language and simulate on Xilinx-ISE system edition design suite 14.1 and also calculate the power consumption using X-power analyser tool of simulation software. This paper shows the comparison with the existing mechanism in terms of on chip power consumption, hierarchy power consumption and clock domain power. This mechanism shows the better results as compare to the existing once.

Keywords: AMBA, ASB, AHB, APB, HDL, Verilog, Xilinx-ISE, SOC, J-K Flip Flop.

I. INTRODUCTION

The feature size of method technology is scaled down day by day. Whereas coming up with a block or associate belongings of SOC, specific set of recommendations need to be planned. As architectures of SOC are shifted to advanced style approaches, a lot of complexities get introduced into the planning concerns and power consumption introduced into image [1]. So, the rules ought to be planned in such how that it provides less integration efforts and helps to the designers for planning a flourishing SOC with a well-structured and synthesizable RTL code with economical in energy and optimized in power consumption.

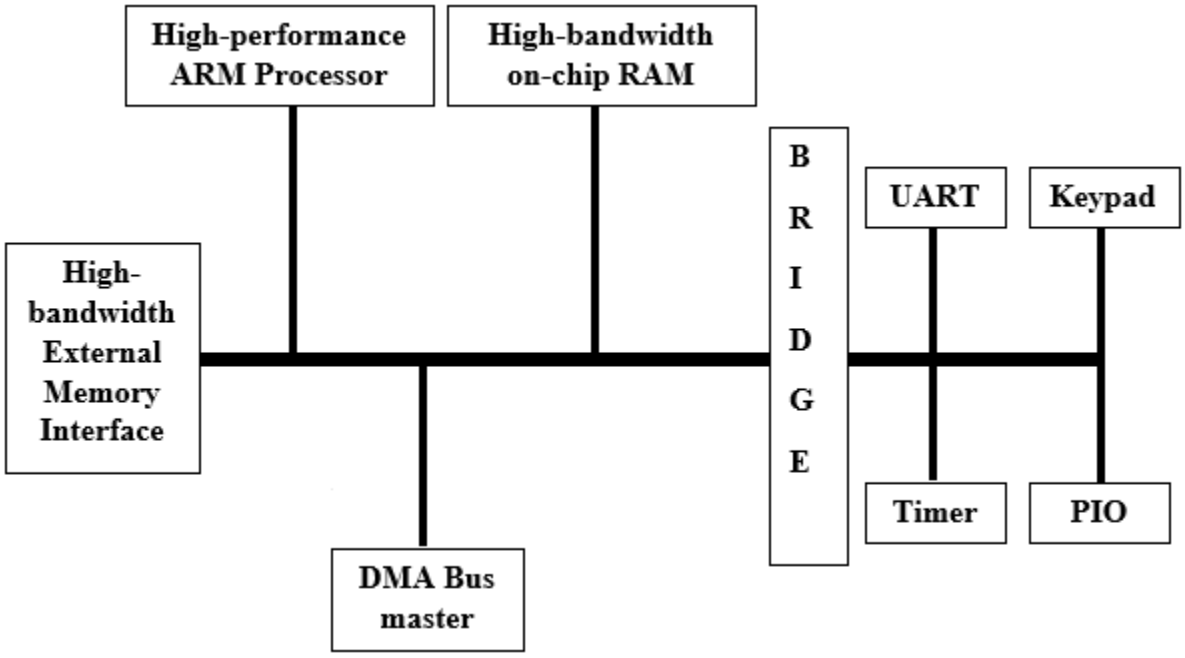

Figure 1: Basic Block Diagram for AMBA Bridges

AMBA that is understood as advance microcontroller bus design may be known as system on chip style concerns in VLSI domain. Fashionable moveable mobile devices like Smartphone, disc and varied ASIC merchandise cannot even imagine while not AMBA buses (Advanced Microcontroller Bus Architectures). Simple AMBA design set up is as above figure 1.

II. RELATED WORK

Abhijeet Paunikar et al [5]: proposed an editorial. In this proposed paper, we gift the planning of Advanced Peripheral Bus (APB) controller (or APB Bridge). UART as partner APB slave has been hired within the making plans. Linear Feedback shift register (LFSR) module has been enclosed within the UART style for information protection. We have additionally compared APB Bridge fashion well suited with AMBA Specification and APB Bridge style well matched with AMBA 3 APB Specification (v1.0) for power and area constraints are overcome.

Jasmine Chhikara et al [6]: In this proposed article, all fashion devices include smaller realistic blocks known as scheme or module. For effective functioning of the system those modules need to be in set with one another and percentage sources. Downside starts when one module follows absolutely different or completely one of a kind protocol as others and every module has its one of a kind bit rate or baud rate of facts switch which may be either asynchronous or synchronous. The paper takes an instance of I2C protocol and AMBA APB protocol to provide an explanation for the design that defines how understanding is transferred from one protocol to a distinctive. It exploits the flexible protocols of I2C to shape it like minded with APB protocol. The planned design might be a bridge between I2C Master and APB Salve. The information travels from a serial bus (I2C) to parallel bus (APB) to serial (I2C) in set with the character area clock. This bureaucracy a two-manner interface among I2C supported module and APB supported module.

Pranav Kumar et al [7]: In this paper proposed, verifying a posh SOC is hard. The check bench and test cases must be advanced early as those are used for the whole thing from SOC verification to comprehend better insurance on function protocol coverage, if integration and overall performance verification. Time to plug makes early pc code improvement a need. Verification strength-assisted with early laptop code improvement wishes pretty dynamic simulation and emulation technique involves rescue. Firstly, the verification of RTL in machine ecosystem has been reasonably priced with SV/UVM methodologies specializing in reprocess on check bench and check instances beside the verification surroundings around Verification data technology. The reprocess technique in centre, the emulation technique gives sizeable theoretical overall performance benefit over dynamic simulations. In theory, too typically verification corporations get not on time disbursal huge amounts of sometime porting verification infrastructure from one stage of checking out to succeeding. It's susceptible to check bench bugs conjointly. On the far facet the horizontal and vertical re-use version, there may be a requirement of end to finish re-use throughout the appearance and verification drift. This paper explains a widely wide-spread technique to comprehend this end-to-give up reuse in a modern project.

Kiran Rawat et al [8]: Offered an article. In this text offered, the primary project for a fashion engineer is not most effective to style a flourishing SOC with a well-dependent and synthesizable RTL code however also to style it with least expensive in electricity and optimized in energy intake. The purpose of the paper is to put in force AMBA APB (superior microcontroller bus architecture - superior peripheral bus) Bridge with cost-effective guidance of machine assets. For this, simulation and synthetization of the advanced bridge interface is meant which might also offer minimum power consumption and occasional facts degree between AMBA excessive pace ASB and low pace APB buses. Clock could be a prime subject in making plans of any digital consecutive system. Clock skew is brought whilst the distinction is generated between the arrival times of clock signal. One of the strategies to lessen clock skew is ripple counter. One will use 3 bit up or down ripple counter method. APB Bridge with clock skew diminution approach is enforced in the paper the usage of Verilog HDL. For the simulation motive, Model-Sim Version 10.3 has been used. For the synthetization cause, style utilization define and power information Xilinx-ISE style suite, version 13.4 has been used. Power record is delivered for developing better information of the facility usage in any machine. The facility report offers the facility intake outline. Hence, the complete clocks electricity intake is of 0.39 mW, total hierarchy power consumption of 0.57 m Wand general on chip logical electricity intake of 0.113 W are extracted from Xilinx X-Power analyser device whilst APB Bridge is styled or meant or supposed beneath the deliberate design technique.

III. PROBLEM DOMAIN

In this quick, we've got executed the survey of different on-chip protocols in conjunction with their features and architectures. A descriptive evaluation between diverse on-chip protocols is wanted. So we must find out the green protocol as it can successfully transfers block of facts thereby lowering the hardware assets and minimum electricity intake. This may be tested by using imposing the our projected protocol at RTL in HDL and comparing

the identical with other protocols by means of thinking about numerous parameters together with transfer time intake, twine efficiency, valid statistics bandwidth, dynamic energy performance and electricity consumption.

IV SYSTEM DESIGN

The aim of this study is to provide a detailed insight into the characteristics of robust low power consumption of deployment of AMBA APB Bridge for SOC model techniques by comparing the performance of representative techniques from each category against energy consumption, power consumption, operational efficiency using the same source content and perceptibility criteria and to propose a hybrid scheme which is robust against common AMBA APB Bridge implementation.

We proposed a new scheme which applies hybrid approach using energy efficient system resources of AMBA APB Bridge for low power consumption SOC model. The scheme is robust against energy consumption.

- Experiments have been done on this deployment of energy efficient system resources design to test, simulate and show its performance.
- We compare the proposed scheme with the existing scheme in different aspects and discuss the advantages and the disadvantages of our scheme.
- Our approach cultivates an idea of energy conservation which applying a hybrid approach to the proposed scheme. Its advantages are clear and significant.

System design methodology need four essential blocks module.

A. APB Advanced Peripheral Bridge Bus
B. ASB Arbiter
C. Master and Slave
D. Decoder

Generally Advanced Peripheral Bus (APB) Bridge plays a vital role in AMBA architecture plan. The APB Bridge provides address, data and control signal latching for connected peripherals. Two operations; Read and Write transfers are performed in it. Read and write transfers require control signal for making decisions APB Bridge behaves as a master on the APB bus and as a slave on ASB/AHB bus.

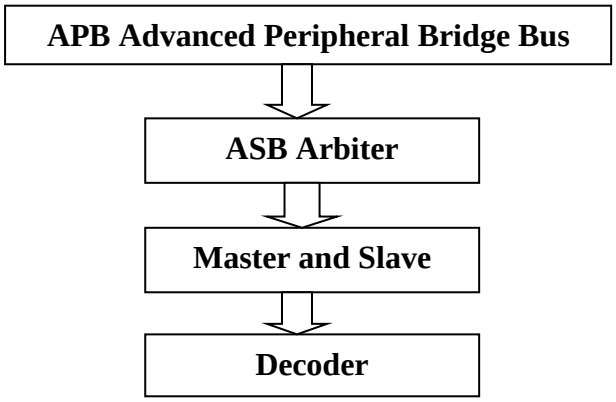

Figure 2: Essential Block Diagram for System Design

V. SIMULATION RESULTS

The synthesis of proposed and resulted design is synthesized with Xilinx Synthesis tool. It is designed with Tcl scripts which run precision RTL synthesis. The RTL views consist of various parts like Master, Slave, Flip-flops and other basic modules as per design as shown in figure 3 and 4.

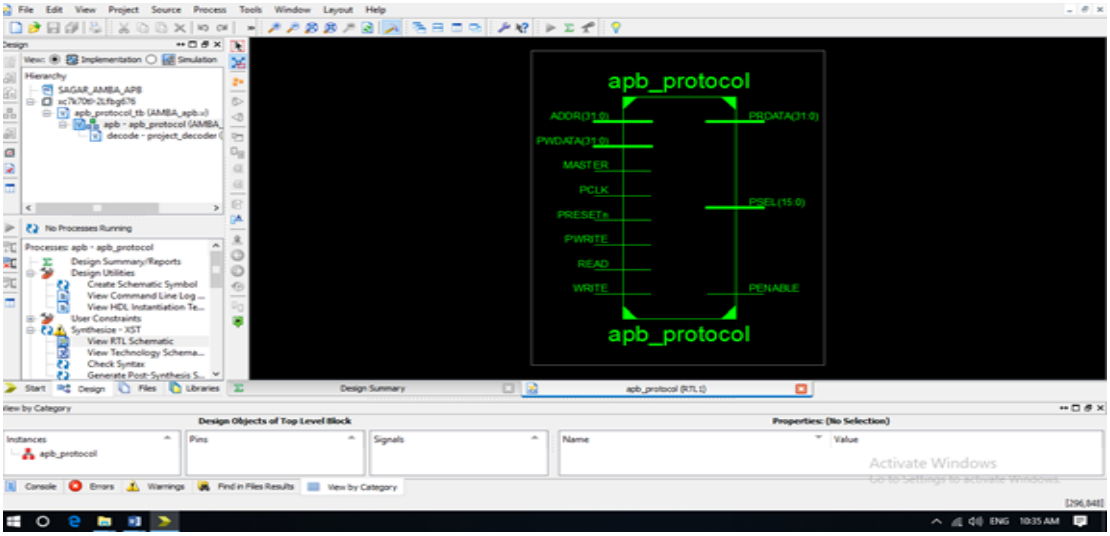

Figure 3: RTL for AMBA-APB

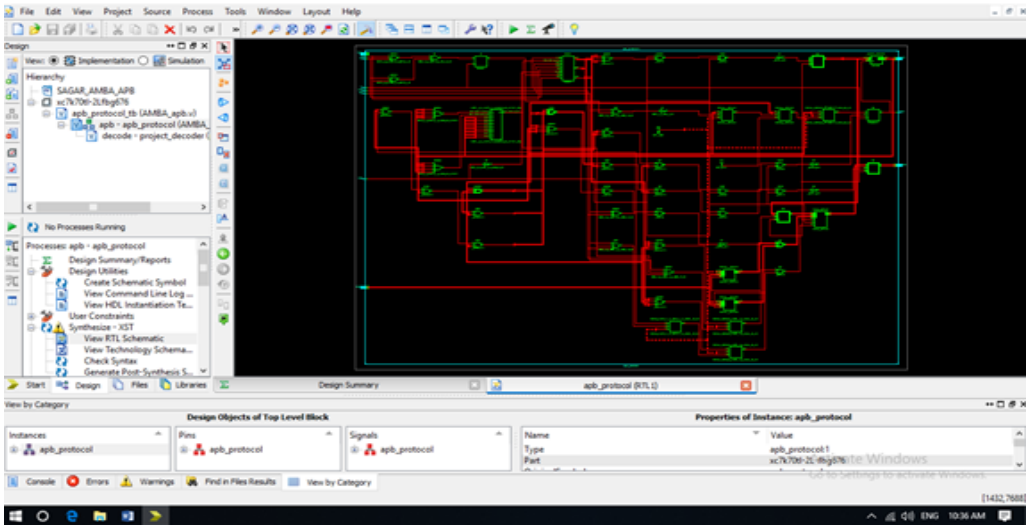

Figure 4: RTL View for AMBA SOC Architecture

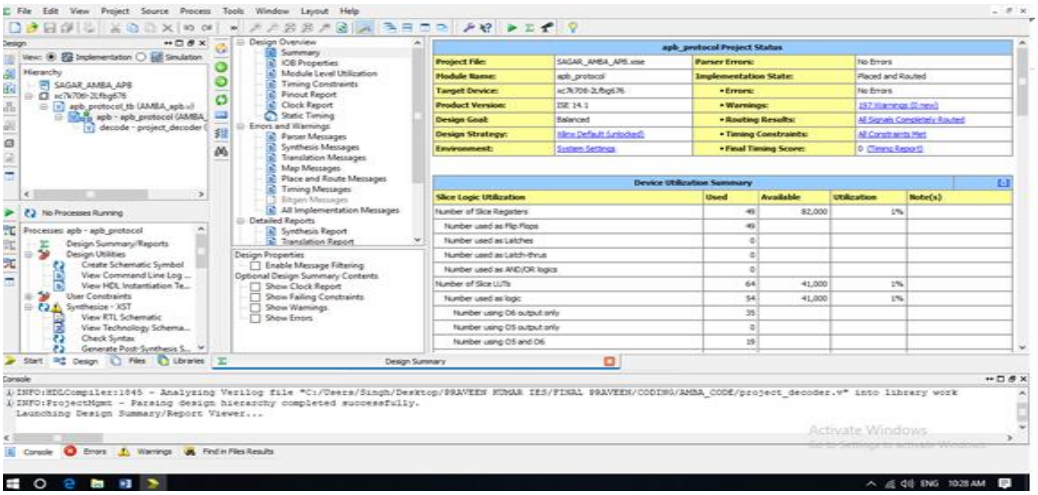

Figure 5: Device Utilization Summary Report

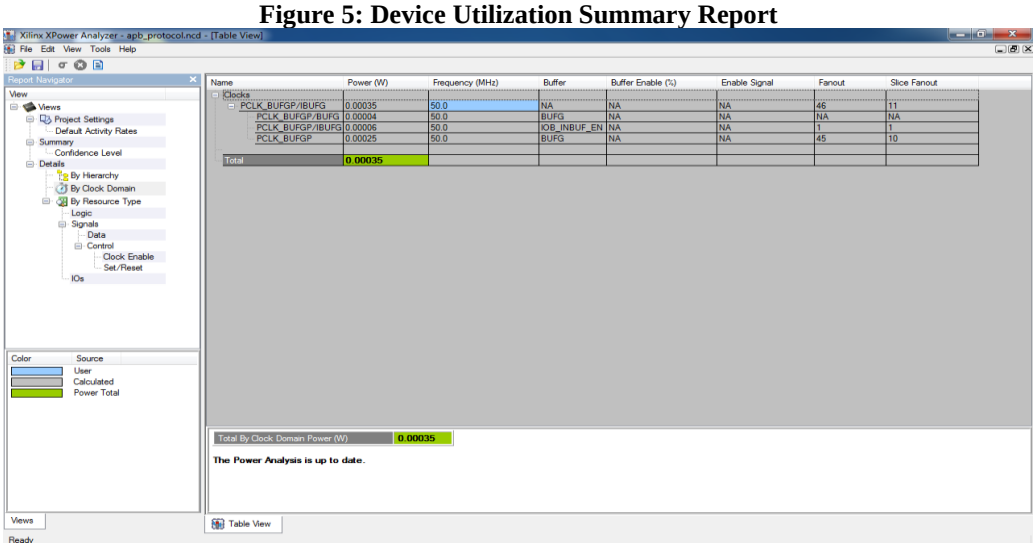

Figure 6: Extracted Power Report for Clock Domain

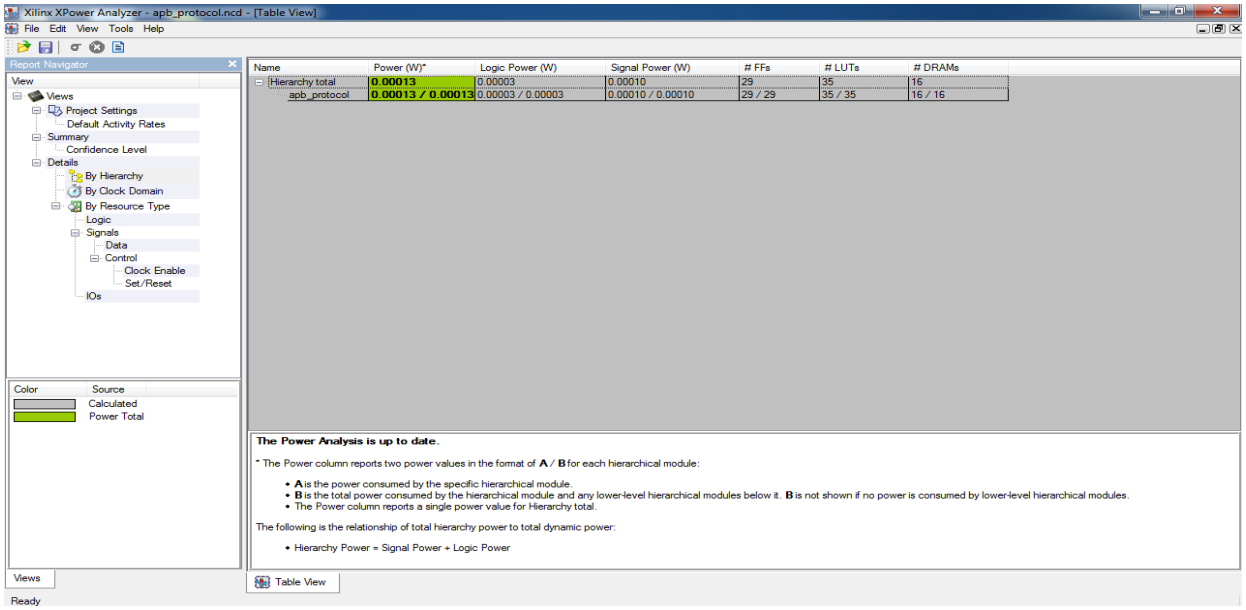

Figure 7: Extracted Power Report for Hierarchy

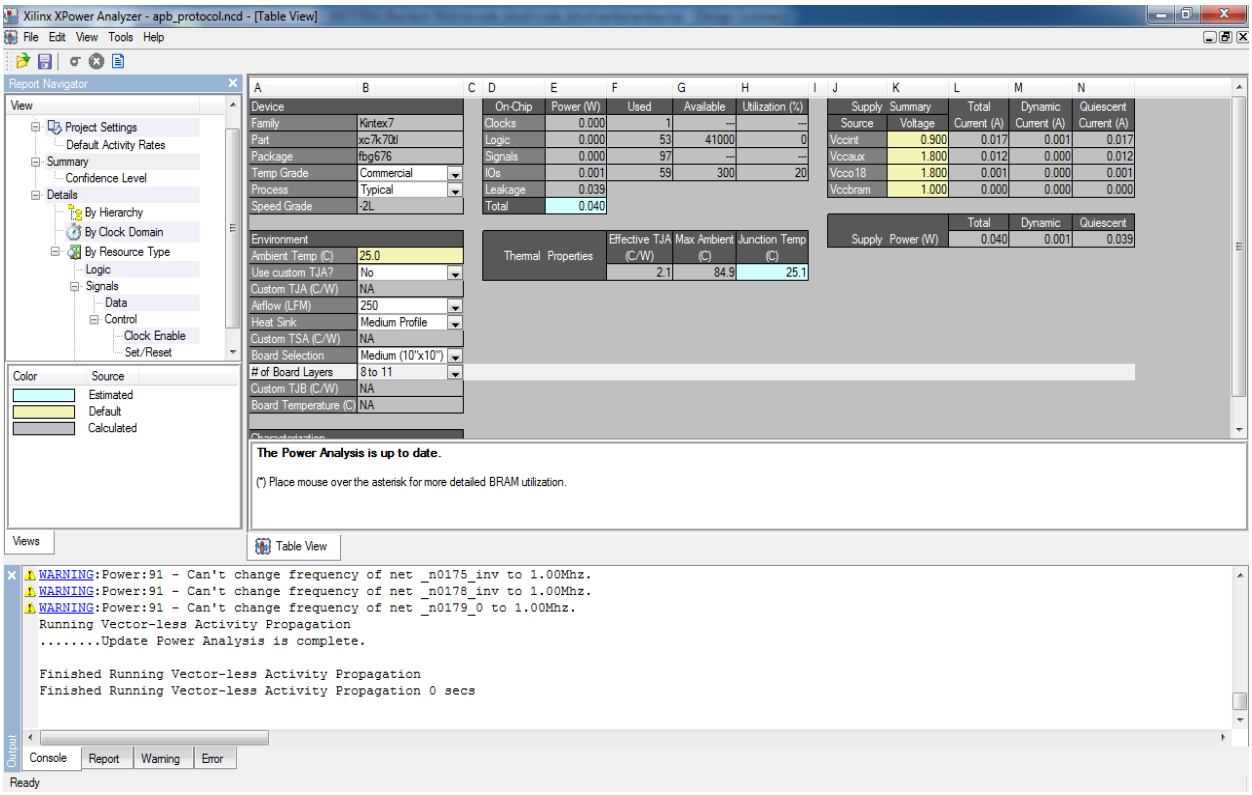

Figure 8: Extracted Power Report for Total On-Chip Power

The objective of the paper has to design an APB bridge with Flip-Flop as a memory element of master slave approach for minimizing the clock skew. Also power reports are included with the proposed design. Unnecessary switching activities of clocks may cause a huge amount of power dissipation around 15% to 50%. Hence proposed design is used to minimize the clock skew and also provides the less power consumption. Clock frequency of 50 MHz and Kintex 7 FPGA family are considered for the virtual hardware implementation purposes as shown in figure 5, 6, 7 and 8.

Table No. 1: Power Report Comparisons between APB Bridge with the Proposed Design Approach (Flip-Flop Master Slave) and Previous Three Bit Ripple-Down Counter Approach

Frequency (MHz)	Power Report of APB bridge with reset controller and three bit ripple down counter approach (W) [8]	Power Report of APB bridge with efficient system resource approach (W)
50	Total Clock Domain = **0.00039**	Total Clock Domain = **0.00035**
	Total Hierarchy Power = **0.00057**	Total Hierarchy Power = **0.00013**
	Total on Chip Power = **0.113**	Total on Chip Power = **0.040**

The variations may be found as:

1. Total clock area strength below proposed design method is decreased via 11% than the preceding bridge layout with reset controller conditions and three bit ripple counter approach.
2. Total Hierarchy electricity below proposed design technique is decreased by way of seventy seven percentage than the preceding bridge layout with reset controller conditions and three bit ripple counter approach.
3. Total on chip power beneath proposed layout approach is reduced via sixty seven percentage than the preceding bridge layout with reset controller conditions and three bit ripple counter approach.

VI. CONCLUSION

In the prevailing paper actually have worked on power reduction and reminiscence green APB protocol implementation. In this dissertation, specifically cantered on using language constraints extra effectively and also use of special capabilities of Verilog for specifying and modelling delays and timings and have worked on concept of using parameterized modelling method which can be beneficial in reuse the layout, enforcing small modules in big designs. The whole clocks energy intake is of 0.35 mW, general hierarchy strength consumption of 0.13 mW and general on chip logical strength consumption of 0.040 W had been extracted from Xilinx X-Power analyser device when APB Bridge is designed beneath the proposed design technique.

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