International Journal of Engineering Technology and Applied Science
(ISSN: 2395 3853), Vol. 3 Issue 2 February 2017

A Literature Review on FPGA Implementation of Image De-noising Techniques

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ABSTRACT- In this survey paper shows the literature survey of different FPGA implementation of De-noising method. Image de-noising is initial task of image processing. Image is often corrupted by impulse noise in the procedures of image acquisition and transmission. There are different filters are implemented in the VLSI, like a decision-tree-based impulse noise detector to detect the noisy pixels, and an edge-preserving filter, mathematical morphological filter etc. These are used to reconstruct of noisy free image pixels. Furthermore, an adaptive technology is used to enhance the effects of removal of fixed valued impulse noise. The performances of different filters are measured in terms of LUTs, IOBs, number of flip flops and also on PSNR, MSE. In this also discuss the different filter FPGA implementation, with the help of FPGA implementation calculate the cost and power efficiency of the different previous methods.

Keywords: IOs, Buffer, flip flops, FPGA, PSNR and MSE

I. INTRODUCTION

Digital image process is an ever increasing and dynamic area with applications reaching out into our standard of living like medication, house exploration, police investigation, authentication, automatic trade examination and plenty of additional areas. Applications like these involve completely different processes like image improvement and object detection. Implementing such applications on a general purpose laptop is easier, however not terribly time efficient as a result of further constraints on memory and different peripheral devices.

Application detailed hardware performance offers abundant larger speed than a software system implementation. With advances in the VLSI (Very large Scale Integrated) technology hardware implementation has become an attractive alternative. Implementing advanced computation tasks on hardware and by exploiting correspondence and pipelining in algorithms yield vital reduction in execution times

Image processing is a wide area with tremendous applications including our everyday life such as medicines, space exploration, military surveillance, image authentication, automated industry inspection, automated control equipment's and many more areas. In most of cases captured images from image sensors are affected by various types of noises. The impulse noise is among one of the most frequently referred type of noise**.**

Median filtering is considered a suitable method to remove impulse noises from images. This non-linear technique is a good substitute to linear filtering as it can efficiently subdue impulse noise while preserving edge information. The median filter operates for each pixel of the image and ensures that it fits with the pixels around it. It filters out samples that are not representative of their surroundings; in other words the impulses. Thus, median filter is very helpful in filtering out missing or damaged pixels of the image..

In addition, throughout design fabrication the presence of one error renders the chip useless. DSPs are a category of hardware devices that fall somewhere between an ASIC and a computer in terms of the performance and also the design complexness.

Field Programmable Gate Arrays are reconfigurable devices. A hardware design technique like similarity and pipelining techniques is developed on a FPGA, that isn't attainable in dedicated DSP designs. Implementing image process algorithms on reconfigurable hardware minimizes the time-to-market value, permits fast prototyping of advanced algorithms and simplifies debugging and verification. Therefore, FPGAs are a perfect selection for implementation of real time image process algorithms. FPGAs have traditionally been organized by hardware engineers employing a Hardware design Language (HDL). The two principal languages used are Verilog HDL (Verilog) and extremely High Speed Integrated Circuits (VHSIC) HDL (VHDL) that permits designers to design at numerous levels of

abstraction. Given the importance of digital image process and therefore the significance of their implementations on hardware to attain higher performance, this work addresses implementation of image process algorithms like median filter, Morphological, convolution and smoothing operation and edge detection on FPGA victimisation VHDL language. Additionally novel architectures for the higher than mentioned image process algorithms are planned. Gray-level images are quite common in image process.

II. Enhancement Techniques

In this section example deferent technics o image enhancement using very large scale integration (VLSI).

Anshan S L, Sowmya C H, Review of An Efficient Object Detection Using System Generator"(2015), This paper basically emphasizes on different methodologies that have been proposed from past few years on object detection. Research on detection has widely covered applications such as artificial intelligence, robotics, security surveillance, identification, face recognition, detection of vehicles in traffic and many more .These applications led to untiring efforts for further techniques yet to be proposed. This paper enlightens us about numerous techniques that have extensively being used for detection in videos [1].

Gurkirat Kaur1, Prof. Rajat Gupta2, Statistical Filter For Removing Noise In Digital Image, 2013,

A Median filter is used for eliminating Salt & Pepper Impulse noise and Wiener filter is used for eliminating Gaussian noise. This paper presents a hybrid filter for removal of both types of noises. Two Hybrid filters are presented for eliminating Salt and Pepper noise and Gaussian noise simultaneously from a noisy image. The first filter is a combination of a variant of Median filter and Wiener filter and the second filter is a combination of a variant of Median, Inverse and Wiener filters. The experimental results show that the second filter is an efficient filter for removal of the two mixed noises in terms of retaining the fidelity of the image [2].

H. Hwang and R.A. Haddad, "Adaptive Median Filters: New Algorithms and Results" IEEE 1995, this method primarily based on 2 kinds of image models corrupted by impulse noise. In this proposed work two new algorithms for adaptive median filters. These have variable window size for removal of impulses while conserving sharpness. The first one, called the ranked-order based adaptation median filter (RAMF), is based on a check for the presence of impulses within the center pixel itself followed by the check for the presence of residual impulses within the median filter output. The second one, called the impulse size based mostly adaptation median filter (SAMF), is based on the detection of the scale of the impulse noise. It is shown that the RAMF is superior to the nonlinear mean L, filter in removing positive and negative impulses while at the same time protective sharpness [3]

S. Zhang and M.A. Karim, "A New Impulse Detector for Switching Median Filet" IEEE 2002, A new impulse noise detection technique for switching median filters is presented, which is primarily based on the minimum definite quantity of 4 convolutions obtained victimization one-dimensional Palladian operators. Extensive simulations show that the planned filter provides better performance than several of the existing switch median filters with comparable procedure quality. In particular, the proposed filter is directed toward improved line preservation. In this proposed work an improved impulse detector that may effectively separate noise and noise-free pixels. In particular, it prevents the removal of fine details such as thin lines from the images and so provides improved impulse detection ability. Both the simulation and procedure quality analysis show that the proposed method is better than several of the existing SM filters such as the median-based, WM-based, ROM-based, and tractate SM filters [4]

III. RESULT PARAMETERS

Number of IOs

Specifies whether or not to infer input/output buffers on all top-level I/O ports of the design. The type of input/output buffer (IBUF, OBUF, and OBUFT) inferred depends on how the port is defined and used in the design. The compiler adds I/O buffers only on ports that do not already have connections to I/O buffers that you instantiate in the design. I/O buffers are required on all top-level ports for the module before it can be implemented. When this property is set to False (checkbox is blank), you must either instantiate I/O buffers on all top-level ports in the design, or you must encapsulate the resulting net list within a higher-level design that contains I/O buffers on all top-level ports before implementing the design.

Number of Silics

Every slice contains four logic-function generators (or look-up tables, LUTs) and eight storage elements. These elements are used by all slices to provide logic and ROM functions. SLICEX is the basic slice. Some slices, called SLICELs, also contain an arithmetic carry structure that can be concatenated vertically up

through the slice column, and wide function multiplexers. The SLICEMs contain the carry structure and multiplexers, and add the ability to use the LUTs as 64-bit distributed RAM and as variable-length shift registers (maximum 32-bit).

Number of Flip Flops

Each slice has eight storage elements. There are four storage elements in a slice that can be configured as either edge-triggered D-type flip-flops or level-sensitive latches. The D input can be driven directly by a LUT output via AFFMUX, BFFMUX, CFFMUX or DFFMUX, or by the BYPASS slice inputs bypassing the function generators via AX, BX, CX, or DX input. When configured as a latch, the latch is transparent when the CLK is Low.

In Spartan-6 devices, there are four additional storage elements that can only be configured as edge-triggered D-type flip-flops. The D input can be driven by the O5 output of the LUT.

When the original 4 storage elements are configured as latches, these 4 additional storage elements can not be used**.**

LUTs

A **LUT** (or Lookup-Table) is basically just a small memory. When you configure the FPGA, you also configure the contents of the **LUT**, and thus the function that you want it to perform. A CLB (Configurable Logic Block) basically consists of a **LUT**, a Flip-flop and multiplexer. In reality, a CLB is a bit more complex though.

The performances of different filters are measured in terms of PSNR, MSE, MAE and RMSE. The whole phenomena are performed on MATLAB and Xilinx.For designing in VLSI used software that is Xilinx xc3s500e-4fg320 FPGA hardware. Also apply finite state machine (FSM). FSM are used to simulate the different algorithms image edge enhancement in Xilinx platform. FPGA is the core part of development of any algorithm with the help of this algorithm sets a level of chip the next stage is testing, testing also a very important part of the result and simulation after the simulation in chip level the stage is testing. There are different tool available for testing purpose on hardware testing as well as software testing available.

Peak Signal to Noise Ratio (PSNR)

Signal to noise ratio is defined by the power ratio between a signal and the background and noise. Where P is an average power. Both noise and power can be measured in a system for same pixel point, and with same bandwidth in system.

$$PSNR = 10\log_{10}\frac{(255)^2}{MSE}$$

Mean Square Error (MSE)

The MSE is the cumulative square error between the encoded and the original image defined by: Where, f is the original image and g is the filtered image. The dimension of the image is m x n. Thus for effective filtering MSE will be as low as possible.

V. CONCLUSION

A low-cost VLSI architecture for efficient removal of random- valued impulse noise is proposed in this paper. The approach uses the decision-tree-based detector to detect the noisy pixel and employs an effective design to locate the edge. With adaptive skill, the quality of the reconstructed images is notable improved. Our extensive experimental results demonstrate that the performance of our proposed technique is better than the An Efficient VLSI Architecture for Removal of Impulse Noise in Image Using Edge Preserving Filter www.iosrjournals.org previous lower-complexity methods and is comparable to the higher-complexity methods in terms of both quantitative evaluation and visual quality. The VLSI architecture of our design yields a processing rate of about 200 MHz by using TSMC 0.18μm technology. It requires only low computational complexity and two line memory buffers. Therefore, it is very suitable to be applied to many real-time applications.

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