International Journal of Engineering Technology and Applied Science

(ISSN: 2395 3853), Vol. 3 Issue 12 December 2017

Review Paper on Various Topologies of Operational Amplifier at 45nm Technology

[1]B. Khandelwal, [2]S. Zafar, [3]J. Mishra

[1]M-Tech Scholar, [2]Associate Professor, [3]Head of Department

[123]Department of ECE, Patel College of Science and Technology, Bhopal, India

[1]bhaskar_khl@yahoo.com, [2]sameena.zafar@gamil.com, [3]jitendra.mishra260@gmail.com

Abstract- In this paper, operational amplifier and its various topologies has been discussed and simulated at 45 nm technology. Operational amplifier topologies operate at a very low supply voltage of 0.7V under the room temperature. Performance parameters such as DC Gain, UGB, Slew Rate, Settling Time, Phase Margin, Leakage current and Power Consumption of various topologies has been simulated, compared and demonstrated. Simulation results show that the multistage OP-AMP is suitable for high gain, high swing and low noise applications. All the simulations have been performed on Cadence at 45nm technology.

KEYWORDS: Telescopic Topology, Folded-Cascode Topology, Multistage Topology, Gain-Boosted Topology, Op-Amp, Slew-Rate

I. INTRODUCTION

An operational amplifier is basically a three terminal device which consists of two high impedance inputs, one called the inverting input marked with a negative sign and the other one called the non-inverting input marked with a positive sign. The third terminal represents operational amplifier's output port which can both sink and source either voltage or current. In a linear operational amplifier, the output signal is the amplification factor known as the amplifier's gain (A) multiplied by the value of the input signal [1]. The amplified output signal of an operational amplifier is the difference between the two signals being applied to the inputs. In other words, the output signal is a differential signal between the two inputs. Standard symbol of operational amplifier is depicted in Figure 1.

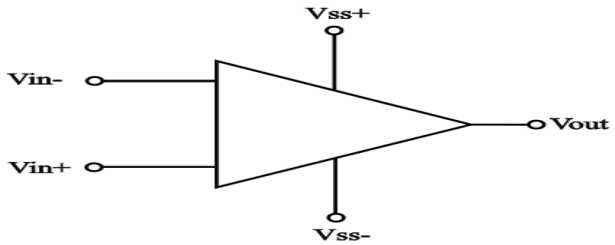


Figure 1: Standard OP-AMP Symbol

The Characteristics of Operational Amplifier may be defined as:

Infinite open-loop gain (Av): The main function of an operational amplifier is to amplify the input signals and the more open-loop gain it has the better. Open-loop gain is the gain of OP-AMP without positive or negative feedback and for an ideal amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.

Infinite input impedance (Zin): Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry. Real OP-AMPs have input leakage current from few Pico amperes to few milli-amperes.

Zero output impedance (Zout): The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load [2]. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output-impedance in the 100-20 Ω range.

Infinite bandwidth (BW): An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GBW) which is equal to the frequency where the amplifiers gain becomes unity [3].

Zero offset voltage (Vo): The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

The small voltage gain of the differential amplifier is found inappropriate for most analog system design. For this reason, operational amplifier is introduced to circumvent the limitations of differential amplifier.

Most operational amplifier architectures employ the differential amplifier as the building block. There are several available operational amplifier architectures. This paper presents various topologies of operational amplifier (telescopic topology, folded-cascode topology, multistage topology and gain-boosted topology) in Section 2. Section 3 elaborates advantages and disadvantages of various topologies. Performance evaluation of various topologies of operational amplifier is presented in Section 4. Simulation Results and Conclusion is presented in Section 5 and Section 6 respectively.

II. TOPOLOGIES OF OPERATIONAL AMPLIFIER

1. Telescopic Topology

The first topology to be described here is a telescopic amplifier topology. Telescopic amplifier topology is used to achieve high DC gain. In telescopic topology, gain is increased by boosting the output impedance of the amplifier. Although, telescopic OP-AMP has smaller voltage swing, which results in reduced dynamic range. The above reason implies that the telescopic OP-AMP is a better candidate for low-power operational amplifier. The telescopic amplifier topology is shown in Figure 2; here, all transistors are biased in saturation region. The input differential pair injects the signal currents into common-gate stages. Then, the circuit achieves the differential to single ended conversion with a cascode current mirror. The transistors are placed one on the top of the other to create a sort of telescopic composition. The small signal resistance at the output node is quite high. It is the parallel connection of two cascode configurations. Such a high resistance benefits the small signal gain without limiting the circuit functionality [4]. The telescopic configuration uses only one bias current. It flows through the differential input stage, the common-base stage and the differential to single-ended converter.

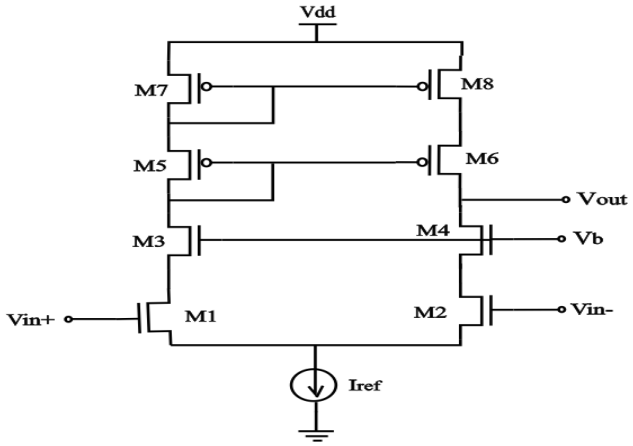


Figure 2: Telescopic Amplifier Topology

Each transistor cascaded on top of another one, adds an overdrive voltage to the headroom of output branch which will limit the output swing. Another drawback is that extra poles are added to the small-signal transfer function of the OP-AMP, exacerbating stability issue [5]. When using this topology, one should be careful about minimum allowable input common-mode level and choosing bias voltages accordingly. At large supply voltages, the telescopic architecture becomes the natural choice for systems requiring moderate gain for OP-AMP.

2. Folded-Cascode Topology

The folded-cascode architecture as shown in Figure 3 is designed to increase the input and output voltage swings. The folded-cascode architecture provides better settling time for small capacitive loads due to its superior small signal response [6]. However, one disadvantage of this architecture is its very low DC gain which is not suitable for high precision application. We saw that telescopic amplifiers suffer from limited output swing. Folded-cascode OP-AMPs allow more swing at the output. Although, this topology consumes more power than telescopic topology due to its need for another current source (M3 and M4 act as a current source).

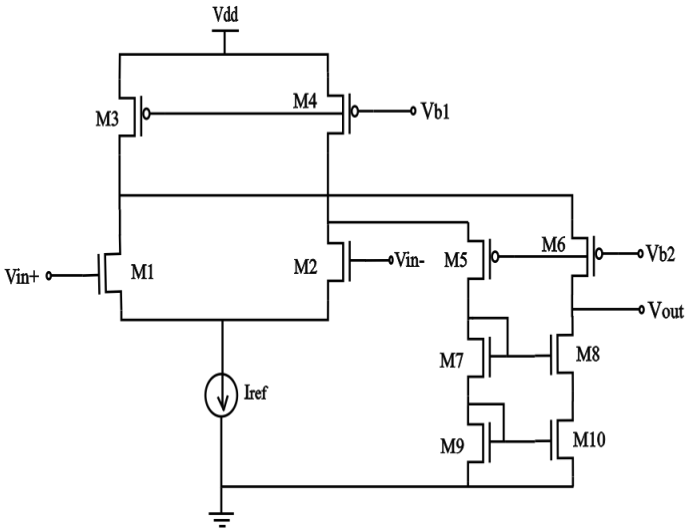


Figure 3: Folded-Cascode Amplifier Topology

Here, the circuit has three stacked devices in the input stage and four in the output stage, giving larger input and output swings than the telescopic amplifier. Although only $V_{ds,sat}$ is needed to saturate the bottom-most load transistors and the top-most current source transistors in order to allow for process variation, a small safety margin V_{margin} is often added to V_{ds} to ensure saturation [7]. An issue that should be kept in mind is that the pole in the source of cascode devices is

closer to the origin than that of telescopic OP-AMP. This issue is exacerbated when using NMOS input devices. The reason lies within the need for larger PMOS transistors, as second current source, to carry both currents of input and cascode devices and obviously larger devices contribute more capacitance. One of the important benefits of folded-cascode OP-AMPs is that their input common-mode level range is larger than that of telescopic OP-AMPs. Depending on the kind of input device, input common-mode level can be very close to one of the supply sources. In case of PMOS input devices, input common-mode level can be zero and having NMOS input device, OP-AMP tolerate input common-mode level equal to V_{dd}. In general the choice of input device depends on the application. Whether gain is the target or common-mode level dictates the input device.

3. Multistage Topology

Multistage topologies can allocate gain and voltage swing in separate stages as depicted in Figure 4, thereby providing viable choices for low voltage design and resistive load drivers. Since Miller capacitors for frequency compensation must be used in multistage topologies, the load driving capacitance is restricted. The high gain requirement for multistage is to use long channel devices biased at low current levels, contradicting the requirement for a high slew-rate. The most widely used circuit approach for the implementation of operational amplifiers is the two stage configuration. This configuration consists of a differential amplifier as the first stage, a current source load inverting amplifier as the second stage, and a Miller compensation capacitor Cc. Both of the DC gain and the gain bandwidth product (GBW) of the circuit are found to be related to the bias current and the sizes of input transistors. Although, both of these parameters can be increased by using larger device area, the trade-off between the DC gain and gain bandwidth product has to be made by varying the bias current [8]. These relationships thus provide flexibility in meeting the desired performance.

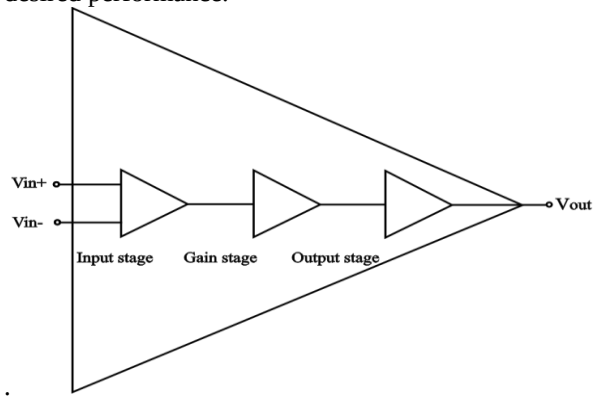
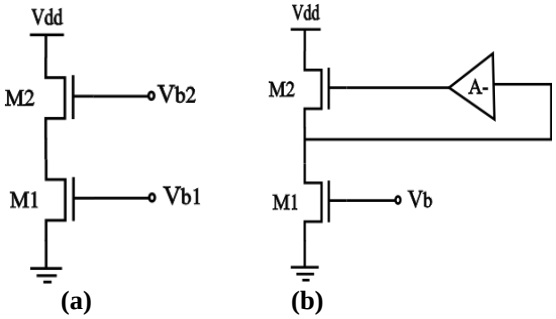


Figure 4: Multistage Amplifier Topology

The principal drawback of this architecture is the degradation of the settling behavior resulted from the non-dominant pole formed by the output impedance and the load capacitance. This implies that the capacitive loading is limited and relied on the compensation capacitor. Furthermore, the effect of the right half-plane (RHP) zero resulted from feed-forward through Cc often requires other circuit techniques to ensure stability [9]. In precision applications involving large open-loop gain, this configuration may be inadequate. More gain can be obtained by appending cascode transistors to the first stage, second stage or both. The result is that the incremental gain of the circuit is equal to the open-loop gain of the cascode transistors. However, in applications where dynamic range is the primary concern, two-stage topology has its own merit. The first stage can provide a high gain, while the second stage is designed for rail-to-rail output swing [10]. The other approach, which is well known but not commonly employed, for achieving high gain is cascading amplifier stages. Though, unlike the cascode topology, this approach does not suffer the reduction in voltage swing, the frequency response is degraded as each cascade stage introduces an additional pole. This problem is alleviated by the nested Miller compensation structure which utilizes Miller capacitors that are connected from the output node of the amplifier to the inputs of the subsequent internal amplifier stages, and thus, non-dominant poles are splinted apart.

4. Gain-Boosted Topology

In telescopic and folded-cascode topologies, increasing output impedance has been used as a means of increasing gain. In both topologies, stacking more transistors in output branch as cascode devices helps to do so. The idea behind gain boosting is to increase the output impedance and achieve higher gain without adding more transistors to the output branch [11]. In this approach, the cascode device is placed in a current-voltage feedback using an amplifier. The limited gain in single stage topology and the low bandwidth associated with multi stage architecture have resulted in the need for the development of gain boosting techniques.



(a) Simple Cascode Circuit, (b) Gain-Boosted Circuit
Figure 5: Gain-Boosted Amplifier Topology

The principle of this topology is to add a feedback amplifier to the cascode device as shown in Figure 5 (b), yielding an output impedance approximately a times larger than the simple cascode circuit of Figure 5 (a), where A is the open-loop gain of the feedback amplifier. This amplifier tends to maintain the drain voltage of M1 by adjusting the gate voltage of M2. In other words, if there are changes in the drain current at the output, the amplifier varies the gate voltage of M2 such that the change in the drain voltage is minimized. The gain boosting topologies can be used in high gain and fast settling operational amplifier designs [12].

III. ADVANTAGES AND DISADVANTAGES OF VARIOUS OP-AMP TOPOLOGIES

Advantages of Telescopic Topology

- Telescopic amplifier topology is used to achieve high DC gain.
- Telescopic OP-AMPs have high speed as the input device's current flows directly into output impedance.
- This topology is simple and there is only one current source in it, so they dissipate power less than other topologies.

Disadvantages of Telescopic Topology

- Telescopic OP-AMP has smaller voltage swing, which results in reduced dynamic range.
- Another drawback is that extra poles are added to the small-signal transfer function of the OP-AMP, exacerbating stability issue.

Advantages of Folded-Cascode Topology

- Folded-Cascode amplifier design has corresponding superior frequency response than multistage operational amplifier.
- It has better high frequency power supply rejection ratio (PSRR).
- The power consumption of this design is approximately the same as that of the two stage design.

Disadvantages of Folded-Cascode Topology

- Folded-Cascode OP-AMP has two extra current legs and thus for a given settling requirement, they will double the power dissipation.
- The folded-cascode architecture also has more devices, which contribute significant input referred thermal noise to the signal.

Advantages of Multistage Topology

- Multistage topologies can allocate gain and voltage swing in separate stages, thereby providing viable choices for low voltage design.
- Multistage OP-AMP is suitable for high gain, high swing and low noise applications.

Disadvantages of Multistage Topology

- The principal drawback of this architecture is the degradation of the settling behavior resulted from the non-dominant pole formed by the output impedance and the load capacitance.
- For multistage topology (especially for more than two stages), the stability problem is undesirable.

Advantages of Gain-Boosted Topology

- The principal advantage of gain-boosted topology is high DC gain without adding more transistors to the output stage.
- The gain boosting topology can be used in fast settling operational amplifier designs.

Disadvantages of Gain-Boosted Topology

- Power consumption of gain-boosted OP-AMP is higher than other topologies.
- The level of complexity of gain-boosted architecture is also high.

IV. PERFORMANCE COMPARISON OF OP-AMP TOPOLOGIES

To accomplish the most competent design of operational amplifier, a comparison of performance of various amplifier topologies is presented in Table 1. As observed from Table 1, a multistage OP-AMP is suitable for high gain, high swing and low noise applications. Whereas for multistage topology (especially for more than two stages), the stability problem is undesirable. As per the design requirements, two stage CMOS OP-AMP is best suited. In two stage CMOS OP-AMP, the first stage provides high gain and the second stage provides large swings. As compared to the cas-code OP-AMPs, a two stage OP-AMP isolates the gain and swing requirements [13].

Table 1: Comparison of Performance of Various OP-AMP Topologies

Parameters	Gain	Speed	Power Consumption	Output Swing	Noise
Telescopic	Medium	Highest	Low	Low	Low
Folded-Cascode	Medium	High	Medium	Medium	Medium
Multistage	Highest	Low	Medium	Highest	Low
Gain-Boosted	High	Medium	Highest	Medium	Medium

V. SIMULATION RESULTS AND DISCUSSION

The design and optimization of OP-AMP topologies is carried out at a power supply of 0.7 V under room temperature in Cadence Virtuoso tool. Performance summary of various OP-AMP topologies is reported in Table 2. As observed from Table 2, multistage OP-AMP is suitable for high gain (82 dB), high unity-gain bandwidth (150 MHz) and adequate phase margin (60º) whereas telescopic OP-AMP provides low power consumption (50 µW). The folded-cascode architecture provides better settling time (95 ns) due to its superior small signal response. The principal advantage of gain-boosted topology is high DC gain (79 dB) without adding more transistors to the output stage. Power consumption of gain-boosted OP-AMP (81µW) is higher than other topologies.

Table 2: Performance Summary of Various OP-AMP Topologies

Performance Parameters	Telescopic OP-AMP	Folded-Cascode	Multistage OP-AMP	Gain-Boosted OP-AMP
DC Gain (dB)	60	62	82	79
UGB (MHz)	95	98	150	105
Slew-Rate (V/µs)	6.9	5.2	10	8.7
Settling Time (ns)	80	95	115	100
Phase Margin (degree)	40	55	60	57
Power Supply (V)	0.7	0.7	0.7	0.7
Leakage Current (pA)	23.7	27	30	42
Power Consumption	50	67	70	81

VI. CONCLUSION

In this paper, various topologies of operational amplifier (telescopic topology, folded-cascode topology, multistage topology and gain-boosted topology) has been discussed and simulated at 45 nm technology. Operational amplifier topologies operate at a very low supply voltage of 0.7 V under the room temperature. Performance comparison of various topologies of operational amplifier is also demonstrated. Simulation results confirm that the multistage OP-AMP is suitable for high gain, high swing and low noise applications. The principal drawback of this architecture is the degradation of the settling behavior resulted from the non-dominant pole formed by the output impedance and the load capacitance. Telescopic amplifier topology is used to achieve high DC gain but it has smaller voltage swing. Folded-Cascode amplifier design has corresponding superior frequency response than multistage operational amplifier. The gain boosting topology can be used in fast settling operational amplifier designs. Power consumption of gain-boosted OP-AMP is higher than other topologies and the level of complexity of gain-boosted architecture is also high. As

per the design requirements, two stage CMOS OP-AMP is best suited.

ACKNOWLEDGEMENT

This research work was supported by ITM University, Gwalior and PCST, Bhopal with alliance of Cadence Design System, Bangalore, India.

REFERENCES

[1] R. J. Baker, "CMOS Circuit Design, Layout and Simulation," Wiley Interscience, New York, 2005.

[2] P.A. G.Sankarand K. U.kumar, "Design and Analysis of Two Stage OperationalAmplifier Based on Emerging Sub-32nm Technology," Proceedings of the IEEE International Conference on Advanced Nanomaterials& Emerging Engineering Technologies,pp. 587-591, 2013.

[3] B.H. Soni and R.N. Dhavse, "Design of Operational Trans-conductance Amplifier using 0.35 μm Technology," International Journal of Wisdom Based Computing, vol. 1, pp. 28-33, 2011.

[4] E. Sackinger and W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit," IEEE Journal of Solid-State Circuits, vol. 25, pp.289-298, 1990.

[5] R. Eschauzier and J. Juijsing, "Frequency Compensation Techniques for Low-Power Operational Amplifiers," MA: KluwerAcademic Publishers, Boston, 1995.

[6] S. M. Mallya and J. H. Nevin, "Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier," IEEE Journal of Solid-State Circuits, vol. 24, pp 1737-1740, 1989.

[7] R. E. Vallee and E. I. El-Masry, "A Very High-Frequency CMOS Complementary Folded Cascode Amplifier," IEEE Journal of Solid-State Circuits, vol. 29, pp. 130-133, 1994.

[8] K. N. Leung, P. K. T. Mok, W. H. Ki and J. K. O. Sin, "Three Stage Large Capacitive Load Amplifier with Damping Factor Control Frequency Compensation," IEEE Journal of Solid-State Circuits, vol. 35, pp. 221-230, 2000.

[9] G. Palmisano, G. Palumbo and S. Pennisi, "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers," Analog Integrated Circuits and Signal Processing, vol. 27, pp. 179-189, 2001.

[10] K. N. Leung and P. Mok, "Analysis of Multistage Amplifier-Frequency Compensation," IEEE Transactions on Circuits and Systems, vol. 48, pp. 1041-1056, 2001.

[11] F. Schlogl, H. Dietrich and H. Zimmermann, "Operational Amplifier with Two-Stage Gain-Boost", Proceedings of the 6th WSEAS International Conference on Simulation, Modelling and Optimization, Lisbon, Portugal, pp. 482-486, 2006.

[12] S. A. P. Mahalingam, M. Mamun, L. F. Rahman and W. M. D. W.Zaki, "Design and Analysis of a Two Stage Operational Amplifier for High Gain and HighBandwidth," Australian Journal of Basic and Applied Sciences, vol. 6, pp. 247-254, 2012.

[13] S. Bandyopadhyay, D. Mukherjee and R.Chatterjee,"Design of Two Stage CMOS Operational Amplifier in 180nm Technology with Low Power and High CMRR,"International Journal of Recent Trends in Engineering & Technology, vol. 11, pp. 239-247, 2014.