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A Literature Review on Energy Efficient Full Adder Design

[1]Bhagyalaxmi Patsariya, [2]Susmita Bilani, [3]Dilip Ahirwar, [4] Prof. R. S. Pandey
[1]M-Tech Scholar, [23]Assistant Professor, [4]Principal
Department of ECE, Adina Institute of Technology, Sagar
{bhagyalaxmi.patsariya26@gmail.com, dilip.adina@gmail.com}

Abstract- The major design constraints in adder design are area and power dissipation. The power dissipation in MOSFET is directly proportional to the output load capacitance and it is inversely proportional to the supply voltage, transistor gain which in turn depends on the switching frequency, sub threshold leakage and switching time. In this paper, we have presented the literature on coming up with of high speed, less area full adder using economical techniques. The optimization of the projected style can be done by using the various techniques. The parameters speed and area of the projected style can be improved by using Carry Look Ahead Techniques. It also reduces the circuit quality. The full adder is a fundamental building block of central process unit of a laptop that is employed within the simplest microprocessors for purpose of maintaining timers. Previously, much economical design has been introduced for the style of low quality operation, but we tend to have given the attention to the carry look ahead and reversible gate techniques.

KEYWORDS: Energy Efficient Design, FA, CLA, Complexity, Area.

I INTRODUCTION

Day by day IC technology is obtaining a lot of advanced in terms of style and its performance analysis. A faster style with lower power consumption and smaller space is implicit to the trendy electronic styles. Full adder usually have extended latency, large space and consume substantial quantity of power. Thence low-power full adder style has become a very important part in VLSI system style. Everyday new approaches are being developed to style low-power full adder at technological, physical, circuit and logic levels. Since the full adder is mostly the slowest part during a system, the system's performance is set by performance of the multiplier. Conjointly full adder designs are the foremost space overwhelming entity during a style. Therefore, optimizing speed and space of a full adder may be a major style issue today. However, space and speed are typically conflicting constraints in order that rising speed leads to larger areas and vice-versa. Conjointly space and power consumption of a circuit are linearly related to. Thus a compromise has got to be exhausted speed of the circuit for a bigger improvement in reduction of space and power.

A higher illustration base effectively indicates to fewer digits. Embedded systems style focuses on low Power dissipation and system-on-chip. A reliable on-chip communication customary is a must in any SOC. This section provides an informative review regarding the designing existing mechanism of full adder combinational circuit.

Energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e. electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e. magnetic field energy, into the digital circuit. If one relates the signal change to the conversion of electric energy to magnetic energy the so-called "energy-recovery" can be realized. This is the method by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e. resistors, is largely reduced or avoided. The energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic and various domino logics. However, those circuits still rely on DC power, and the energy conversion remains as electric energy to heat. There is need for further study in the case of circuits supplied with AC power. The AC power controls the working rhythm of the circuit and acts as the clock, called the power-clock.

The research shows that the adopted power clock with gradually changing process during its rising and falling dissipates only less energy for charging and discharging the node capacitance through the conducting of MOS transistor. The "adiabatic" switching operation is resulted, by which a new approach to design low power CMOS circuits is proposed. Clocked CMOS circuits with gradually rising and falling power-clock were expected to obtain a significant energy saving. It attracts many researchers to study this issue in recent years. However, the operational constraint that the output signal should track the power clock's gradually rising and falling behavior to accomplish the charging and discharging process increases the difficulty in the circuit design. At present, the existing research either adopts retractile cascade power clock or adopts multiple phase power clock with memory schemes.

The new research on the energy recovery CMOS circuit should start from its basic theory, including the basic algebraic expressions and the basic properties of clocked signals. At the same time, both the basic clocked CMOS gate and the clocked flip-flop, the basic unit of energy recovery CMOS circuits, should be investigated at the beginning. With the above view this research will focus on these two topics.

A variety of full adders using static and dynamic logic styles has been reported in literature, 34 of which have been stated by (Jiang et al 2008) alone, including the most well-known static complementary CMOS adders using 28 transistors and 40 transistors.

II LITERATURE SURVEY

The research [1] introduce that the full adder cells play a vital role in numerous VLSI circuits. Therefore, design of an energy-efficient full adder which operates reliably in submicron technologies has become a great concern in recent years. Some previously designed cells suffer from non-full swing outputs, high-power consumption and low speed issues. In this paper, two high-speed, low-power and full swing full adder circuits are designed in 90-nm CMOS technology. According to simulation results, the proposed circuits have rail to rail output signals. Also, an improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay, power consumption and power-delay product (PDP), respectively.

In this paper [2], hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve Low power and high speed. Hybrid logic style used is the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The Circuit was implemented using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA) and Transmission Function adder (TFA). Average Power consumption of the proposed design is found to be 1.114 µW at 90nm for 1.2V supply and 5.641 µW at 180nm for 1.8Vsupply. Delay in the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies respectively. Thus consuming extremely low power and requires less time than existing designs for the same testing environment. Power Delay Product (PDP) is calculated as product of Power and delay values signifies energy requirement of the design. Proposed design requires 71% less energy than TFA and 81% less energy than TGA and 92% less energy than conventional CMOS adder.

The research article [3] proposed that the designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is array multiplier. Array multiplier half adder have been used to sum the carry products in reduced time. Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier, which is the major power consuming element in the digital circuits. Basically the process of multiplication is realized in hardware in terms of shift and add operation. The optimization of adder has led to the improvement in performance of multiplier. In this paper, a modified full adder using multiplexer is proposed to achieve low power consumption of multiplier. To analyze the efficiency of proposed design, the conventional array multiplier structure is used. The designs are developed using Verilog HDL and the functionalities are verified through simulation using Xilinx. The ASIC synthesis results of the proposed multiplier shows an average reduction of 35.45% in power consumption, 40.75% in area, and 15.65% in delay compared to the existing approaches.

In modern nanotechnology and quantum computation [4], reversible logic plays a pivotal role as it has minimal impact on physical entropy. Reversible logic gates have same number of input and output hence power loss due to bit erase operation can be avoided. There are many reversible logic structures which can perform different Arithmetic and logic operations as traditional or classical logic structures can do. In this paper, two reversible logic structures are proposed which can perform operation of addition. These logic structures namely proposed design I and Proposed design II, generate carry output signal and carry propagate signal on the basis of two reversible logic gates known as Fredkin gate and Feynman gate. Performance of proposed designs is evaluated in terms of quantum cost, constant input, garbage output and delay. It is found that proposed design II is a better choice over proposed design I and some other existing Designs.

The Paper [5] discussed the comparative analysis of different Fin-FET based full adder cells designed with various logic styles. The logic styles used for implementation of Fin-FET based 1-bit full adder are Complementary MOS (CMOS), Transmission Gate (TG) and Complementary Pass-Transistor Logic (CPL). The simulations have being done at 10nm, 20nm and 32nm technology node for all full adder cell designs. PTM models for multi-gate transistors (PTM-MG) low power are used for simulations. The performance parameters that were measured, analyzed and compared are average power, leakage power, delay, and energy. It is observed that less power is consumed in Transmission Gate (TG) based full adder than the Convention full adder and complementary pass-transistor logic (CPL) based full adder in 10nm technology node. Also, found reduction in delay, EDP, and PDP in TG based full adder compared to other cell designs.

The paper [6] very large-scale integrated circuit (VLSI) design, based on today's CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based design can resolve the issue of leakage power and bring the advantage of non-volatility. However, radiation-induced soft error is still an issue in such new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike regardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. They also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full non-volatility for future nonvolatile microprocessors.

The research [7] introduce the solution of the serious problem of threshold loss that causes non-full-swing at the out-put of 1-bit full adder, an arrangement in which all the transistors are forced to operate in sub-threshold regime is proposed in this paper. But this will in turn bring additional area and delay overhead. In this work, full swing at the output of 1-bit full adder is retained with reduced area and delay overhead. An additional capacitor working in the differential voltage mode will be replacing the transistor that is used to reduce the threshold loss problem at the output of 9T based full adder as discussed in this paper. Previous works related to this domain concerns about reduction of power of only 1-bit adder. The work targets power and area reduction of 1/4/8/16 bit adders. Proposed adder shows maximum total power saving of 46.87 % and 25.99 % with respect to 8T and 9T adder configurations respectively.

This paper [8] present, a three transistor XNOR gate. The proposed XNOR gate is designed using CADENCE EDA tool and simulate using the SPECTRE VIRTUOSO at 180 nm technology. The proposed results are compared with the previous existing designs in term of power and delay. It is observed that the power consumption is reduced by 65.19% for three transistor XNOR gate and 48.11% for eight transistor full adder. It is also observed that the delay is reduced by 31.82% for three transistor XNOR gate and 28.76% for eight transistor full adder.

This paper [9] proposes the design of a low power, high speed, and energy efficient full adder using modified Gate Diffusion Input (GDI) and Mixed Threshold Voltage (MVT) scheme in 45nm technology. The proposed design on comparison with the traditional full adder composed of CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), respectively, exhibited a considerable amount of reduction in terms of average power consumption (Pavg), peak power consumption (Ppeak), delay time, power delay product (PDP), energy delay product (EDP) as well as transistor count and hence surface area. Pavg is as low as 7.61x10-7 watt while Ppeak is as low as 6.21x10-5 watt, delay time is found to be 2.05nano second while PDP is computed to be as low as 1.56x10-15 Joule and EDP is evaluated to be as low as 3.20x10-24 Js for 0.9 volt power supply. The simulation of the proposed design has been performed in HSPICE and the layout has been designed in Micro-wind.

In this paper [10] they have designed the full Adder using hybrid-CMOS logic style by dividing it in three modules so that it can be optimized at various levels. First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. It also consumes minimum power and provides better delay performance. Second module is a sum circuit which is also a XOR circuit and uses carry input and the output of the first module as input to generate sum output. Third module is a carry circuit which uses the output of the first stage and other inputs to generate carry output. In the new full adder design we have proposed new full adder circuit which reduce the power consumption, delay between carry out to carry in and PDP by 12 to 100%. Simulations are carried out on HSPICE using TSMC 0.18 μm CMOS technology.

III PROBLEM STATEMENT

Performance factors such as power, delay, and layout area were evaluated with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS output drive full adder. Due to toughness beside CMOS scaling and transistor sizing with the overhead of high input capacitance and requirement of buffers, the adder using this static CMOS. Also this design proves the power dissipation cause due to the stray capacitances and large length interconnects. The circuits design using CMOS logic with large number of transistors and maximum length interconnect are gradually more existing provider to propagation delay, overall area and power consumption. The main goal of this work is to improve the different function parameters such as power dissipation, path propagation delay and number of transistor used in full adder design compared with the previously existing ones.

Floating point (F.P.) addition is a preferable operation for a wide range of applications. The main areas in which they work are area-efficient, dynamically configurable, multi precision architecture for F.P. addition. In our work the use of transmission gate decreases the number of transistors which overcomes the area tradeoffs. The main drawback of the parallel adder is that the delay rises linearly with the bit length. Hence planned design will have:

- How circuit components get integrate?
- How to design and implement Dynamic CMOS gates and a set of experiments and results considering the features of the implemented gates.
- Representation of wiring connectivity in adder circuit.
- Presentation of every gate level property like truth table.
- Representation of connectivity of gates.
- For floating point numbers we design a power and area efficient adder.
- To overcome slow speed of a parallel adder and propagation delay of the carry.
- The main drawback of the parallel adder is that the delay rose linearly with the bit length.

IV CONCLUSION

The efficient module of the full adder has been mentioned. After totally learning these literatures we have a tendency to have concluded that the techniques that non-heritable are far more effective to enhance the parameters of designed module of full adder. These help in optimizing the system by using economical techniques. The full adder design using transmission gates and reversible logic gate approach will increase the speed to an excellent extent but it will increase the hardware complexness. Also, we efforts will be directed towards implementation of full adder style with totally different circuit topology and optimization.

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